



DESIGN A LOW-NOISE 5GHZ WIDEBAND MICROWAVE POWER AMPLIFIER USING 90NM CMOS TECHNOLOGY WITH AREA REDUCTION EMPLOYING AN ACTIVE INDUCTOR

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ABSTRACT

Systems that rely on wireless technology frequently use radio frequency integrated circuits (RFICs). Modern wireless communication systems rely heavily on low-noise amplifiers, particularly those operating in the 5 GHz frequency spectrum using 90nm technology. Improving the performance of 5 GHz low-noise amplifiers is the goal of research into these devices, which tries to solve problems with noise, gain, and power efficiency. When designing better, more efficient, and more balanced wireless communication systems, low-noise amplifiers are a must-have component. This research study introduces a 5 GHz wideband low-noise amplifier (LNA) for 5G Wi-Fi applications. A 1.2 V power source powers it. The circuit features an optimized common source topology to lower the noise figure, which in turn increases the voltage gain and reduces power consumption. To ensure that the circuit is compatible with the source impedance, methods such as inductive source decomposition and single-stage common source decomposition are employed. The mathematical analytical method was incorporated into the design process and served as its fundamental element. The results showed that with a transistor width of 165 μm and a current flowing through the circuit of 4 mA, (NF = 1.266) a gain of 18.493 dB S (2,1) and a power consumption of 4.8 mw were achieved. In terms of achieving a balance between the results of noise and gain, we were unable to accomplish the essence of the design process through mathematical analysis. Since a satisfactory outcome cannot be achieved through mathematical analysis, we optimise using the genetic algorithm. This method is known for its high efficiency in establishing a gain-noise balance and yields effective optimization solutions. We got these results: With an NF of 1.308



and an ideal power usage of 2.64 mW, we achieved an optimal gain of 27.21 dB(S_{21} , 1). Our results show that evolutionary algorithms greatly improve LNA performance by pointing to the best settings for maximizing gain and reducing noise. Lastly, this work illustrates how genetic algorithm optimization has drastically changed LNA design. Engineers can accomplish RF signal amplification feats never seen before by integrating state-of-the-art computational tools and modelling methodologies. Since these methods successfully satisfy the demanding requirements of modern wireless communication systems, the findings indicate that RFIC technology is heading in the right direction.

KEYWORDS

LNA, NF, RFIC, GA, MOGA, 5G Wi-Fi APPLICATIONS CMOS technology.

1. INTRODUCTION

In intricate wireless communication networks, radio frequency integrated circuits (RFICs) serve as the brains. These analogue circuits are renowned for their exceptional efficiency and run at 5 GHz. (Abdo, E., Younis, A. and Ismael, A., 2020). The low-noise amplifier (LNA) is the initial member of a family of radio reception components that enhances weak signals from antennas with the lowest possible noise level. Finding the sweet spot between gain, noise level, and power consumption is crucial, even when designing a low-noise signal amplifier. (Manjula, S., Suganthi, M., Anandan, P., & Pown, M. (2024). Achieving the ideal balance between signal gain and noise reduction has proven to be a significant issue in the design process of low-noise amplifiers (LNAs), which must balance power consumption and noise coefficient (Das, P. and Jajodia, B., 2022). A major source of difficulty is the intricate web of interdependencies between the numerous design parameters and how they impact the circuit's operational efficiency. An optimization technology known as a genetic algorithm was employed to circumvent this problem. This algorithm takes its cues from biological evolution, which involves iteratively generating solutions and then evaluating them using a fitness function that indicates their proximity to the ideal solution. (Singh, V., Pattnaik, S. and Gupta, S., 2017). The most promising offspring inherit mostly their parents' traits with a few tweaks here and there from each generation that follows. Values of electronic components and circuit characteristics stand in for each potential solution inside the amplifier design. Solutions that produce a higher gain with a lower noise level will be given a higher value by the fitness function. This evolutionary process is repeated for multiple generations, allowing the algorithm to thoroughly explore the design space and reach near-optimal solutions. The width of the transistors M1, M2, and M3 is reduced and algorithmic constraints on the inductors are added to facilitate the optimization process on the genetic algorithm. (Chrisvin, D. S., Dharshini, M., Senthilkumar, S. N., & Sundari, T. J. V. (2022, March).). Using ADS software, we simulate the electronic circuit properly to check the performance as shown in Fig.1. The optimization features available in MATLAB are used. Based on experimental results, it's plausible that 90nm technology produces more noise and higher gain than 180nm technology. On the other hand, 90nm technology has other benefits, such as a shrinking chip area. An active inductor can be used when a single-ended amplifier is operating by modifying it so that it can reduce low-frequency noise. This noise can come from anywhere, including other components in the circuit or even outside of it. It is possible to create an active inductor with a restricted bandwidth, allowing the amplified signal to flow through it while reducing noise outside of that frequency range. While active inductors can offer potential benefits such as reducing chip area and improving

performance in certain scenarios, their application in low-noise amplifiers requires careful design and analysis. For example, the noise performance of active inductors can introduce additional noise, especially at higher frequencies. It is essential to analyze the noise figure of the amplifier to ensure that the active inductor is not causing a deterioration in the overall noise performance. Gain, especially at higher frequencies, is enhanced by this as well.

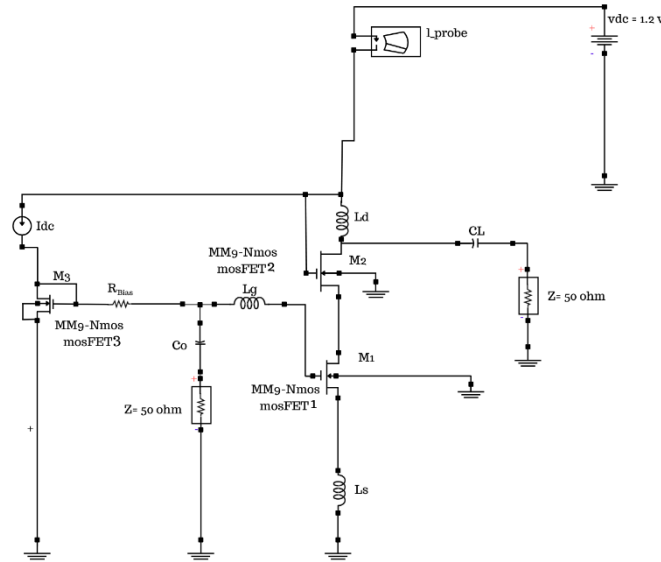


Fig.1. Single-Ended LNA

1.1. Aim of the study Through

Using genetic algorithms, this research aims to contribute to the development of LNA circuits strategy to keep pace with developments in the field of communications and improve the circuit operation by employing it to obtain amplification of weak signals and work to reduce noise during the amplification process while reducing power consumption.

1.2. Background

Researchers have explored many approaches to address this challenge. Genetic algorithm-based approaches have been widely applied in circuit optimization. Researchers have demonstrated the effectiveness of these algorithms in reducing power consumption. In 2023, Rasheed, Israa Mohammed, and Hassan Jasim Motlak research focuses on the design and analysis of low-noise amplifiers (LNAs), that have a vital role in the functioning of communication systems. This research delves into the difficulties of CMOS technology in particular to find solutions to the problems of low noise and high gain in LNAs. The paper goes over a number of methods for designing circuits, such as using serial codes and common sources, and stresses the significance of matching inputs and bias circuits. The findings show that whilst existing methods like inductive source degeneration work. (M. S. Maktoomi, A. Jha, and S. Hamid,). In 2022, Sharma, Nitika, Kaur and Dhaliwal's The front end of the WuRx rotary receiver is

designed and implemented with an 868 MHz low-noise amplifier (LNA) as its primary focus. The objective is to make WSNs better by making each sensor node do more, particularly in terms of lowering latency and power consumption. The rapid reaction times and little power consumption of WuRx nodes have garnered a lot of attention. Impedance matching, stability, power consumption, noise profile, and balance are key design problems. (N. Sharma, S. Kaur, and B. S. Dhaliwal (2022)).

In 2023, the paper by Li, Zeng, Yuan, He, Fan, Tan, and Yu analyzes the primary constraints on low-noise amplifiers' (LNA) ability to expand their bandwidth, and develops a wideband LNA that can operate within the frequency range of 2-40.5 GHz. Several techniques for increasing the LNA's bandwidth were used into its design, including as the Darlington cascade amplifier, resistive feedback, and cascade code. We theoretically study the three structures' frequency and amplitude properties, as well as their bandwidth expansion concept, using the small signal equivalent circuit model. The utilization of 0.15 μm GaAs technology with pseudo-high form electron mobility (PHEMT) allowed for the development of a three-stage LNA amplifier. (Li, J., Zeng, J., Yuan, Y., He, D., Fan, J., Tan, C. and Yu, Z., 2023).

2. LOW-NOISE AMPLIFIER

2.1. Basic Low Noise Amplifier Realization and Topologies

Realization and Topologies of Simple Low Noise Amplifiers. The research examines several low-noise amplifier circuit designs, each with unique benefits and drawbacks that give analog circuit designers a versatile toolkit to tailor the amplifier to specific application needs. Two fundamental topologies that are examined are the differential and single-ended low-noise amplifier designs. Because of its simple functioning and simplicity of integration into compact, single-chip circuits, CMOS technology dominates the production of low-noise amplifiers. (Bruynsteen, C., 2023). To get the best possible design for a single-ended, narrow-band, low-power, low-voltage, low-noise amplifier, as illustrated a few fundamental investigations are needed. This study looks into several different topologies, including common-source with inductive degeneration, cascaded common-source with feedback, common-gate, common-source with resistive terminations, various loading schemes, and cascade with source load. (M. S. Maktoomi, A. Jha, and S. Hamid,). Designers can carefully develop an amplifier that precisely fits within the application's restrictions by carefully examining these configurations.

2.2. Inductive source degeneration cascade in a single-ended LNA device

By choosing the right inductance value, the true part of the input resistance in this innovative design is accurately regulated. A second transistor, M2, is utilized in a cascade setup to enhance

isolation between the tuned input and output. The mutual influence between the tuned circuits is lessened as a result of this configuration. (Rasheed, I. M., & Motlak, H. J. (2023)). The clever arrangement of transistors M1 and M3 to create a current mirror is utilized in the construction of the bias system. In order to guarantee the bias function's lowest power usage, (M3) was carefully enhance the efficiency of power transfer to the output, a L_d inductor is employed to produce frequency with the external load. Actually, the ability of an LNA to amplify signals with the least amount of extra noise and the best power consumption is determined by the perfect coordination of components and their interactions. (Kumar, N., & Bisht, R. (2020, November)). The Fig.1 depicts the schematic diagram of a single-ended low-noise signal amplifier. It shows how an inductor, designated L_s , is strategically connected to the transistor's source terminal. The amplifier's noise and stability properties are improved by this technique, which is referred to as inductive source damping. In communication systems, electronic transmitter and receiver circuits are used to transfer data to and from a designated communication medium. On the receiving end, there are issues that do not present on the sending end. or feel incredibly comfortable. The communication channel's properties are the main source of this, as they result in a minimum detectable signal at the receiver input that could be as low as a μ Volts. To ensure a reliable flow of information, the receiver must be equipped to handle such a signal. (Han, C., Deng, Z., Shu, Y., Yin, J., Mak, P. I., & Luo, X. (2023)) The receiver's sensitivity, or its ability to detect a weak input signal, is effectively limited by the electrical noise at the receiver input.

3. SYSTEM AND DESIGN

3.1. Mathematical Results of Single Ended LNA at 5 GHz with 90nm technology

It is imperative to maintain the original meaning of the fundamental elements while implementing precise values to guarantee adherence to the fundamental performance characteristics criteria. MOSFET transistors with the labels W1, W2, and W3 are size-optimized during the design development process. Another part of this is figuring out the values of the inductances for the drain (L_d), gate (L_g), and loss (L_s). Along with selecting appropriate conductance capacitance values, such as input capacitance (C_0) and load capacitance (C_2), the design also entails determining the correct bias current (I_d), while ensuring that the component portions of the circuit have consistent values. The circuit for the simplified little signal counterpart, the entrance impedance determined, is likewise shown in a unique way.

$$Z_{in} = R_g + \left(\frac{g_m}{C_{gs1}} \right) L_s + j \left(\omega L_s - \frac{1}{\omega C_{gs1}} \right) \quad (1)$$

Eq. 1 can be formulated as follows:

$$Z_{in} = R_g + R_a + j(xL_S - X_{cgs1}) \quad (2)$$

Where

$$R_a = \left(\frac{g_{m1}}{c_{gs1}} \right) L_S \quad (3)$$

The means that the impedance without feedback from the MOSFET will be:

$$Z_{in} = R_g - jx_{cgs1} \rightarrow z_{in} = -j(X_{cgs1}) \quad (4)$$

Changing the input impedance is a crucial step in the design of low-noise signal amplifiers in order to boost efficiency. To harmonize with Cgs, an extra inductor is put in series with Lg. Resonance is achieved by choosing a value for Lg that offsets the influence of Cgs. (R.R.M. AL shaker,). The relationship below provides the input impedance:

$$Z_{in} = \left(\frac{g_{m1}}{c_{gs1}} \right) L_S ; Z_{in} = 50\Omega.$$

Usually, the Id value is determined first, and then the gm and Cgs values are extracted to achieve the desired input impedance Rin. Using 90 nm technology and an operating frequency of 5 GHz, these values are chosen based on the available process specifications. (M. S. Kusuma, Shanthala, and C. P. R. P., (2018)). By adding series feedback, the entry impedance is improved by adding a new term to the original impedance.

$\mu_0=293.168 \text{ m}^2 \text{ V} \cdot \text{s} /$, $C_{ox}=8.221 * 10^{-15} \text{ F}/\mu\text{m}^2$, $\epsilon_0=8.854*10^{-12}$, $\epsilon_r=3.9$ for Sio2, $V_{DD}=1.2 \text{ V}$, $I_d=4 \text{ mA}$, $L=0.09 \mu\text{m}$.

Step1. The width of the MOSFET 1 (M1) MOSFET (M2) transistor device is determined according to reference. (Shuhaimi, A.F.A.F., Amin, N.H.M., Muhamad, M., Hussin, H. and Karim, J., 2021):

$$W_1 = \frac{3}{2 * C_{OX} * L_1 * Q_{OPT} * W_{O * R}} = 165 \mu\text{m} \quad (5)$$

Step2. The Gate to source capacitor Cgs is calculated as. (Yadav, N., Pandey, A. and Nath, V., 2016, January):

$$C_{gs} = \frac{2}{3} * C_{OX} * W_1 * L_1 = 0.0.813 \text{ PF} \quad (6)$$

Step3. Trans-conductance (g_{m1}) of MOSFET1 (M1) is given as:

$$g_{m1} = \sqrt{2 * \mu_n * C_{OX} * \frac{W}{L} * I_d} = 59.45 \text{ ms} \quad (7)$$

Step4. Therefore, the transistor unity gain frequency WT is:

$$W_T = \frac{g_m}{c_{gs}} = 731.3 \text{ Grips} \quad (8)$$

Step 5. The minimum noise figure is given as. (Younis, A. T., & Abdo, E. A. (2020)):

$$NF = \left(1 + 1.62 * \frac{W_O}{W_T}\right) = 1.07 \quad (9)$$

Step 6. Then the voltage gain can be determined as. (H. P. Koringa, 2017):

$$A_V = 20 \log \left(\frac{1}{C_{gs} * W_O * 50} \right) = 17.88 \quad (10)$$

Step7. The values of L_S , L_g , and L_d are obtained as follows:

$$L_S = \frac{R_S}{W_T} = 0.0683 \text{ nH} \quad (11)$$

Where R_S is the input resistance 50Ω

$$L_g = \frac{1}{W_O^2 * C_{gs}} - L_S = 12.4 \text{ nH} \quad (12)$$

$$L_d = \frac{1}{W_O^2 * C_L} = 3.38 \text{ nH} , \text{ where } C_L = 0.3 \text{ pF} \quad (13)$$

Step8. The power dissipation is then calculated to be:

$$P_D = V_{DD} * I_d = 4.8 \text{ mW} \quad (14)$$

Where I_d is the current 4mA.

The LNA component values were derived using computational analysis, and the efficacy of the results was demonstrated through simulation using Radio Frequency (RF) simulation software in the Advanced Design System (ADS). The single-ended amplifier circuit is powered by a 1.2V supply and uses 4.8mW. It is designed in accordance with the 90nm CMOS BSIM3 standard.

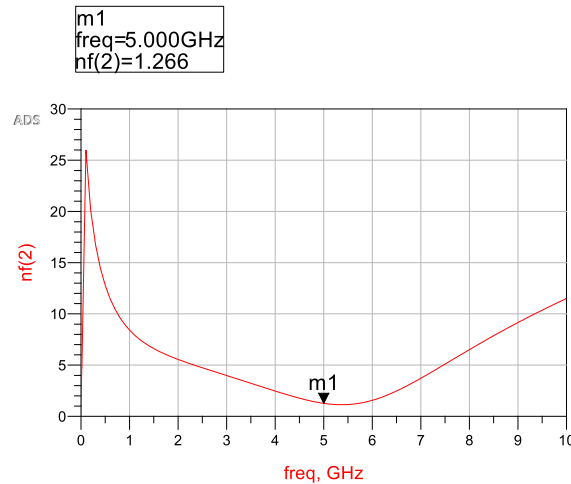


Fig.3. Mathematical NF for 5 GHz Single Ended LNA

This value indicates that the amplifier adds little noise to the input signal. This means that the amplifier maintains signal quality, which is important for use in systems that require high sensitivity. As shown in Fig.3.

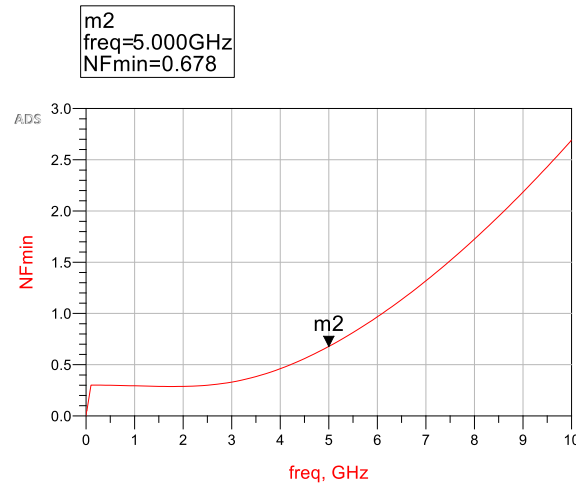


Fig.4. Mathematical Minimum noise figure for 5 GHz Single Ended LNA

The value represents the lowest noise level that the amplifier can generate. It means that the amplifier is able to achieve excellent noise performance under optimum operating conditions. It is an important indicator for applications that require very low noise by providing ideal operating conditions as shown in the Fig.4.

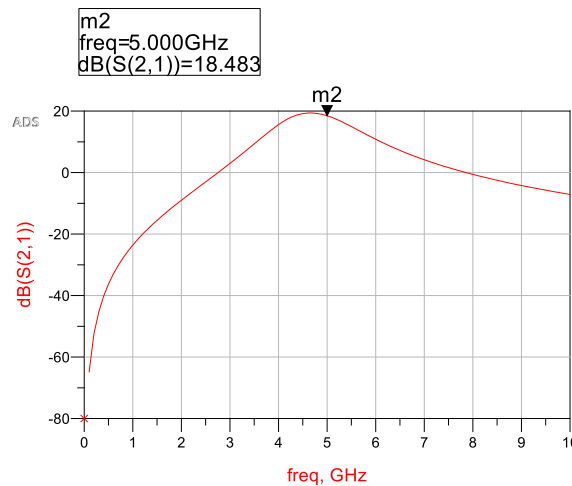


Fig.5. Mathematical Power Gain for 5 GHz Single Ended LNA

This value indicates the amount of signal amplification performed by the amplifier that works to amplify the signal in an acceptable manner in some applications of short-range wireless communication systems as shown in the Fig.5.

A good match between the amplifier, the load, and the source is indicated by the negative values of the reflection coefficients S11 and S22 as shown in Fig.6 and Fig.7. Because of this excellent match, there is less signal reflection, which improves the power transfer efficiency and reduces losses. As a result, the probability of oscillations is reduced and the performance of the amplifier is more stable. This property is very important for many electronic applications, especially those that need to transmit signals efficiently while maintaining their quality, including sensitive receivers and wireless communication systems.

After performing mathematical simulation, the extracted values were successfully obtained.

NF = 1.266, Minimum noise figure=0.678 gain=18.483 and dB (S (1,2)) =-23.458, and dB (S (1,1)) = -24.062, as in Fig. 3, Fig. 4, Fig. 5, Fig. 6 and Fig. 7.

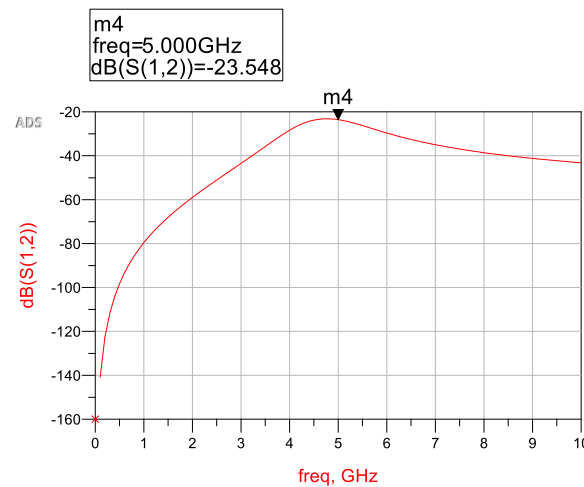


Fig.6. Mathematical Results for Revers isolation for 5 GHz Single Ended LNA

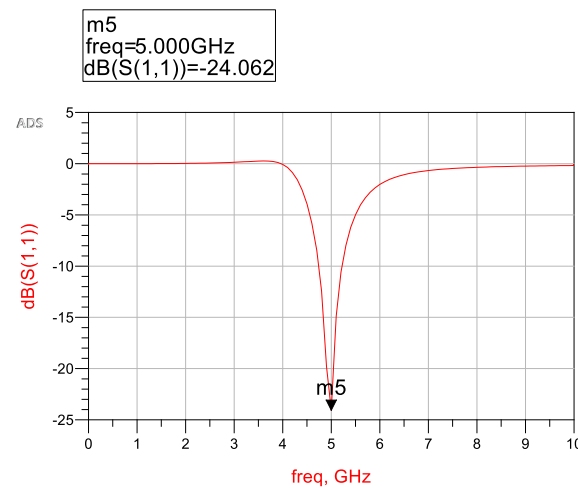


Fig.7. Mathematical Input Return Loss S11 for 5 GHz Single Ended LNA

3.2. optimization Results for Single Ended LNA at 5 GHz

The nanoscale in order to design MOSFET transistors as well as possible, genetic optimization techniques need to be used. Manually determining the values of optimal design variables is highly challenging, if not impossible, due to the complexity of the mathematical models governing these interactions. These difficulties can be overcome and the time required to reach ideal values shortened with the use of optimization techniques. (Fadhil, G., Abed, I., & Jasim, R. (2021)). The importance of genetic optimization techniques in the nanoscale development of MOSFET transistors. Because of their small size, these transistors' electrical activity is highly influenced by quantum events. These complex occurrences require highly developed mathematical models to explain them. Manually adjusting these models to find the best values for design variables like gate length and insulating layer thickness is quite time-consuming.

This is where genetic improvement techniques are applied. Strong algorithms mimic how better designs are selected and "bred," or modified, for greater functionality, similarly to how natural selection works. (Alkafaji, E., & Swadi, H. L. (2024)). By iterating through this process, genetic optimization algorithms eventually arrive at MOSFET designs with the necessary attributes, such as high gain, low noise, and moderate power consumption. When developing radio frequency circuits, engineers have to balance many competing demands. High gain, low noise rates, and energy efficiency must all be combined. The MOGA algorithm is the greatest choice when compared to other approaches because of its greater optimization capabilities and ease of MATLAB implementation. This method allows designers to efficiently enhance the functionality of .

3.3. Optimization for Power Consumption, Noise Figure and Maximization Gain

In the world of loudspeaker design, striking a balance between multiple performance measures can be difficult. Multi-objective optimization (MOGA) techniques provide a powerful way to handle this complexity. For example, power consumption, noise figure, and gain are three factors that all fight for attention while building a low starting point noise amplifier (LNA). Here, MOGA is particularly good at navigating this complex trade-off landscape. Lowering the noise level (noise factor) of your LNA may be required in order to ensure sufficient amplification (gain) and minimal power usage. (Bouali, H., Benhala, B., & Guerbaoui, M. (2023)). This kind of complicated problem could be encountered by traditional optimization methods. This is when MOGA becomes useful. In this case, finding several Pareto optimal solutions can be facilitated by applying the MOGA technique. These solutions are a collection of methods that excel in one area without significantly degrading the others. MOGA enabled the researchers to accomplish this amazing feat with the least number of resources, proving the technique's efficacy in solving extremely difficult optimization challenges. More detailed implementation information of the MATLAB programming environment's MOGA-based optimization process is given in Fig. 8. This figure graphically illustrates the different phases of the MOGA approach, which helps to explain how the algorithm arrives at plausible Pareto-optimal solutions.

4. DESIGN OBJECTIVES AND CONSTRAINT OPTIMIZATIONS OF LNA INDUCTIVE SOURCE DEGENERATION

Chromosome cells in a genetic algorithm are made up of two real numerical values that represent the design variables (width $W1$ and I_d), and Table 1 lists the limitations pertaining to these variables.

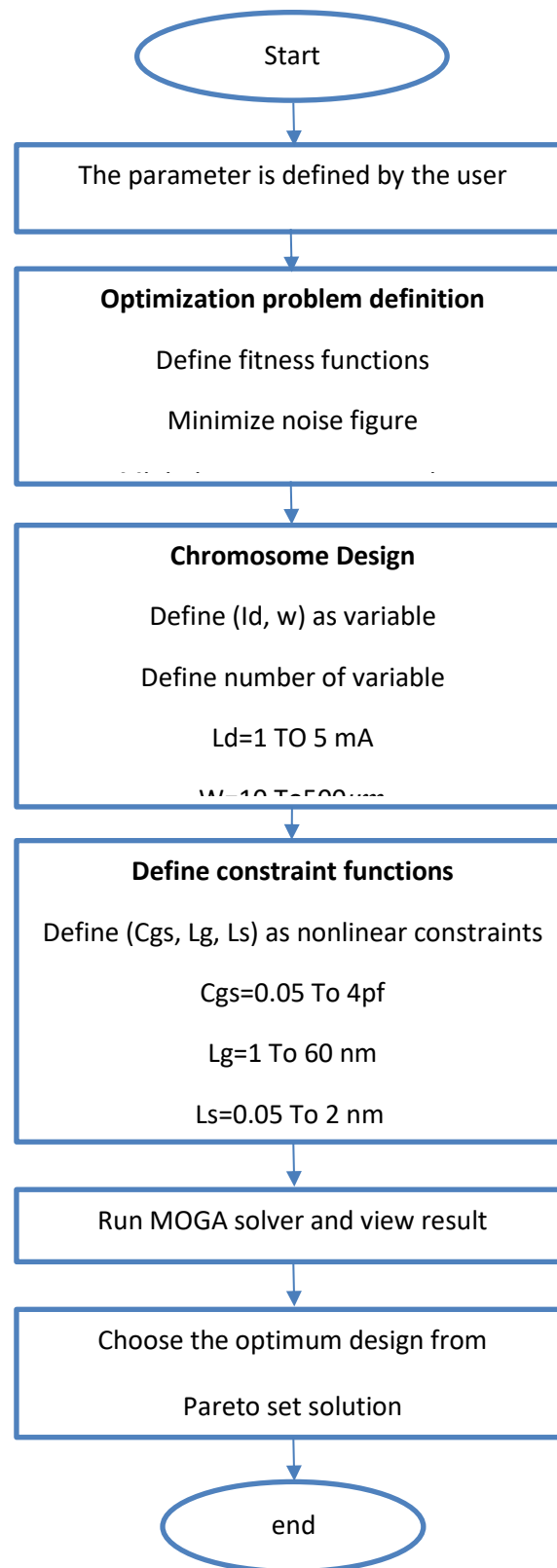


Fig.8 Flowchart of Genetic Algorithm Procedure Based on MATLAB

Table 1: Design Variables and Constraints Limit Using MOGA

VARIABLE'S NAME	CONSTRAINTS VALUES
I_D	1 TO 5 MA
W_1	10 TO 500 μ M

Table 2: Constraints Limit Using MOGA

PARAMETER	CONSTRAINTS VALUES
C_{gs}	0.05 TO 4 PF
L_S	0.05 TO 2 NH
L_G	1 TO 60 NH

Table 3: LNA Specifications Design Target for 0.09 μ m CMOS Process

PARAMETER	VALUE
FREQUENCY (GHZ)	5
SUPPLY VOLTAGE(V)	1.5
S_{11} (DB)	< -10
S_{21} (DB)	> 15
NOISE FIGURE (DB)	< 2
POWER CONSUMPTION (MW)	<8
SOURCE/LOAD IMPEDANCE (Ω)	50

The MATLAB MOGA optimization tools make use of the low noise amplifier's performance parameters. Some of these factors were used as constraints, but other parameters were taken into account when developing the recommended fitness functions. [Table 4](#) gives an overview of these specifications.

Table 4: Design Constraints and Specifications for Low Noise Amplifier

SPECIFICATIONS/CONSTRAINTS	TYPE	EQUATION
GAIN	Fitness Function	10
NOISE FIGURE	Fitness Function	9
POWER DISSIPATION	Fitness Function	14
GATE TO COURCE CAPACITOR C_{GS}	Constraint	6
L_S DEGENERATION INDUCTOR	Constraint	11
L_g INDUCTANCE AT THE GATE	CONSTRAINT	12

Table 5: Optimal variables value of proposed LNA

COMPONENTS	OPTIMIZATION METHOD
WIDTH W_1 (μ M)	71.8
I_d (MA)	2.2
C_{gs} (PF)	0.0354
L_g (NH)	28.58
L_S (NH)	0.061
POWER CONSUMPTION(MW)	2.64

5. SIMULATION OPTIMIZATION RESULTS FOR SINGLE ENDED LNA OF 5 GHZ.

We see a minor rise in the noise value following the genetic algorithm-based optimization

procedure, as depicted in the Fig. 9. There are a number of reasons for this, but the primary one is that 90nm technology is more complicated than 180nm technology. Consequently, lowering the transistor width using 90nm technology increased the circuit's operational complexity, which in turn caused some circuit elements' noise values to slightly increase. This, in turn, caused the ultimate noise value to slightly increase.

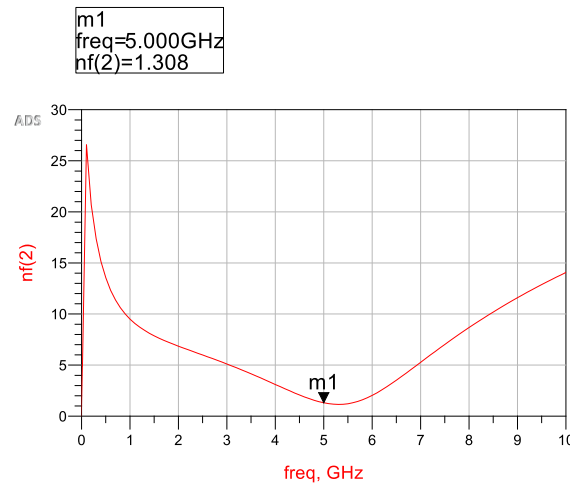


Fig.9. Optimization NF for 5 GHz Single Ended LNA

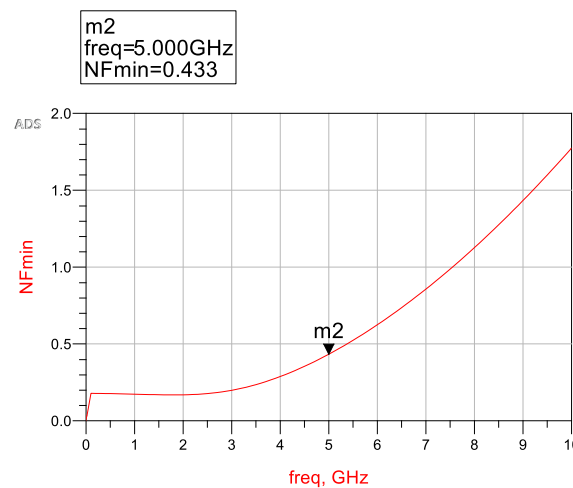


Fig.10. Optimization for Minimum noise figure for 5 GHz Single Ended LNA

It can be seen that following the optimization procedure, the lowest noise dropped, as shown in the Fig. 10. This shows that, under ideal circumstances, the algorithm is successful in lowering the overall noise by establishing a match in the circuit and, ideally, handling the transistor values and electromagnetic interference.

As seen in Fig. 11, the gain dramatically increased during the optimization procedure, reaching 27.210dB. The algorithm balanced the values of the circuit elements and enhanced the amplifier's internal stages, which is why this is the case. To take advantage of all the values of the components that go into creating the circuit, this is crucial.

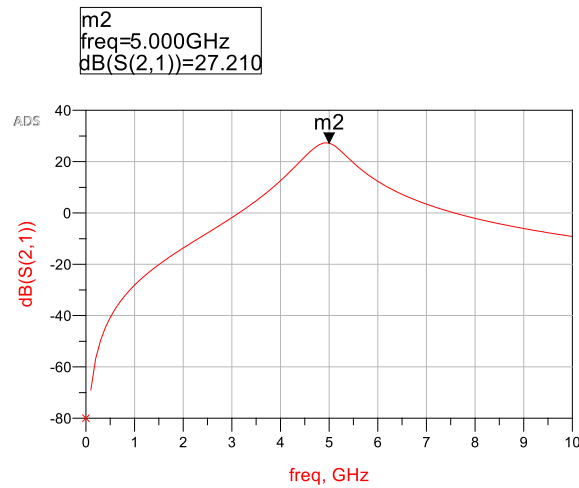


Fig.11. Optimization Power Gain for 5 GHz Single Ended LNA

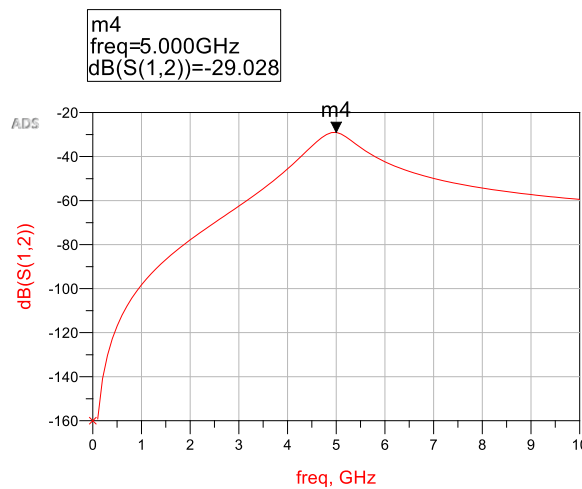


Fig.12. Optimization Results for Revers isolation for 5 GHz Single Ended LNA

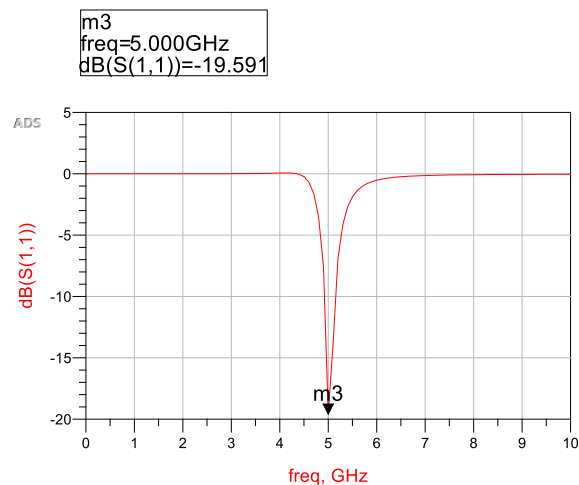


Fig.13. Optimization Input Return Loss S11 for 5 GHz

As seen in Fig. 12, the (dB S1,2) value dramatically increased, suggesting either a decrease in noise at high frequencies or an improvement in voltage gain at those frequencies. On the other hand, a change in the input capacitance caused the (dB S1,1) value to slightly worsen, as seen in Fig.13.

6. COMPARISON BETWEEN MATHEMATICAL AND OPTIMIZED RESULTS FOR SINGLE ENDED LNA AT 5 GHZ

When comparing the low-noise amplifier design in Table 6 using the genetic algorithm and the traditional mathematical method, the results showed that the genetic algorithm was clearly superior in obtaining the optimal performance. Significant gains in amplifier gain and noise handling were achieved by this method, demonstrating its exceptional ability to comprehensively explore the solution space and reach optimal values for the engineering parameters. This superiority can be explained by the evolutionary algorithm's ability to adapt to various design constraints and its versatility in dealing with complex situations. Its evolving nature, which draws inspiration from biological evolutionary methods, also allows it to adapt to changing conditions and provide creative solutions.

Table 6: Comparison between optimization technique and the analytical method

Design Parameters and Performance	Single Ended Low Noise Amplifier	
	Mathematical	Optimized using GA
Width $W1(\mu\text{m})$	165	71.8
$I_d(\text{mA})$	4	2.2
$C_{gs}(\text{PF})$	0.0813	0.0354
$LS(\text{nH})$	0.0683	0.061
$L_g(\text{nH})$	12.4	28.58
$L_d(\text{nH})$	3.38	5
NF(dB)	1.266	1.308
Power Consumption(mw)	4.8	2.64
Gain(dB)	18.483	27.210

7. COMPARISON BETWEEN THE OPTIMIZATION TECHNIQUE OF ADS AND OTHER EXISTING LITERATURE

The adoption of the improvements resulted in an improvement in the quality of the design, as demonstrated by a comparison of the indicated references with the findings of a comprehensive study of the analytical approaches and improvements utilized in the research presented in Table 6. After comparing the amplifiers with references [24], [25], [26], and [27], it can be concluded that the suggested $0.09\mu\text{m}$ diameter low-noise amplifier with inductive source damping performs worse in terms of power gain, noise level, and power consumption. These conclusions are corroborated by the data in Table 7. To make comparisons easier, this analysis offers a comparison between the output of this work and other low-noise signal amplifier design strategies.

Table 7: Comparison between optimization technique and the analytical method

PARAMETERS	[13]	[21]	[22]	PROPOSED WORK
TECHNOLOGY	0.09um	0.18um	0.18um	0.09 um
SUPPLY VOLTAGE	1.2 V	0.63 V	0.63 V	1.2 V
FREQUENCY (GHZ)	5	5	5	5
NOISE FIGURE (DB)	1.330	4.3	4.1	1.308
S21(DB)	20.443	14.7	21.4	27.210
POWER CONSUMPTION (MW)	1.91	0.387	0.48	2.64
S11	-12.790	-15.32	-12.7	-19.591

8. CONCLUSIONS

With the aim of achieving superior performance metrics necessary for contemporary wireless communication systems, this work focused on the design and optimization of a low-noise amplifier (LNA) operating at 5 GHz. Advanced computational methodologies and modeling tools were used in the process. Finding the ideal balance between noise figure (NF), gain, and power consumption is often difficult using traditional approaches to designing a low-noise amplifier. Since RF signal amplification is inherently complex, efficient optimization methods are needed. A powerful approach that used evolutionary concepts to iteratively optimize LNA configurations was the development of genetic algorithms, or GAs. GAs search large design regions through simulated natural selection, finding arrangements that optimize signal strength while minimizing noise interference. In order to navigate the complex, nonlinear dynamics inherent in RF circuit design, this evolutionary technique has proven to be quite useful. ADS was used to validate theoretical models in the first simulation results, which showed an LNA performance of 1.266 dB, a gain of 18.483 dB, and a power consumption of 4.8 mW. MATLAB-based GAs were then used to further modify these values to produce an ideal NF of 1.310 dB, a gain of 27.210 dB, and a power consumption of 2.64 mW. These results demonstrated the effectiveness of genetic algorithms in raising LNA performance above conventional limits. Furthermore, this work demonstrated the advantages of embedding high-performance LNAs in integrated single-chip devices using 90 nm CMOS technology. Several LNA circuit topologies were investigated to meet specific objectives including single-ended and differential circuits. Novel approaches including inductive source decomposition were applied to improve stability and noise performance, thereby increasing amplifier efficiency and

reliability in practical applications. Multi-objective genetic algorithms, or MOGAs, allow for optimization of gain, NF, and power consumption while balancing conflicting design objectives. This approach has increased overall efficiency as well as improved the ability of RF integrated circuits (RFICs) to meet the stringent requirements of modern communications systems. We strive Future studies on new optimization strategies, evaluation of different circuit topologies or adding feedback that have a positive impact and increase the stability of the circuit and work on expanding the frequency range. With the increase in the frequency range, we may resort to other manufacturing techniques (45nm, 28nm). All this development in circuit technologies increases the design complexity, so the design process may become more machine learning-based, which will help in increasing the performance of the LNA even more. Continuous progress in computational tools and modeling techniques will inspire RFIC innovation.

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