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OPTIMIZATION OF FREQUENCY SYNTHESIZERS FOR WIRELESS LOCAL AREA NETWORK COMMUNICATIONS

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ABSTRACT

Wireless communications are integral to modern technology, particularly as telecommunications innovations have rapidly progressed over last half of twentieth century. The demand for wireless local area network (W LAN) hardware has surged in recent years, driven by advancements in transmission speeds, coverage areas, security, quality of service (QoS), and mobility resulting from continuous evolution of WLAN technology. A wireless communication system's transmitter architecture, transmission rate, and receiver architecture are all determined by wireless communication channel. Since establishment of IEEE 802.11 protocol, WLANs have undergone significant transformation over past two decades, reflecting the increasing demand for their services. IEEE 802.11 standard specifies physical layer for communication across a local area network that is wireless across frequency ranges of 2.4, 3.6, 5, and 60 GHz. Wi-Fi primarily operates within multiple frequency bands, such as 2.4 GHz and 5 GHz, offering a variety of channels to accommodate multiple devices in diverse environments. This work aims to design a radio frequency synthesizer characterized by high speed and minimal noise. The results obtained show that when it relates to producing high-output signals with little spur noise, the second frequency synthesis that was suggested performs superior. At a 2 MHz frequency offset, the phase measurements of noise for 2.4 GHz register at -155.799 dBc/Hz, and at a 3 MHz frequency offset, they reach -170.596 dBc/Hz, which is within the permitted range. Additionally, synthesizer achieves an improved settling time of 6.320 μs.

KEYWORDS

Wireless Communication, IEEE 802.11 Standard, Wireless Local Area Network, Phase Locked Loop, Frequency Synthesizer, Phase Noise.

1. INTRODUCTION

In contemporary times, Wireless neighborhood network standard IEEE 802.11 has gained widespread usage as an affordable and fast Internet access network. It serves as a flexible alternative to conventional LANs and facilitates data transmission Interpersonal communication, for instance, between different continents and countries has grown readily available, inexpensive, and astonishingly precise. (Choi, 2010; Ali and Hreshee, 2023) The most crucial parts of radio and communications networks are transceivers, which allow the use of wireless communication to expand beyond simple two-way communication to include the distribution of voice, video, and other forms of data over long distances via orbiting satellites. By using using radio frequency technology for data transmission and reception over air, WLAN can reduce requirement for physical connections. Frequency synthesizers are fundamental parts of wireless devices in the efficiency of today's wireless networks as a result of phase noise and spurious content are highly significant since they have first-order effects on transceiver system as a whole. Although there are other frequency synthesizing architectures, most widely used option for producing a reference clock is a frequency synthesizer based on phase-locked loops (PLLs) (Lwin, 2018; Hameed, 2019). Professor Bellescize initially discussed phase-locked loop circuits in 1932; they allowed for the simultaneous reception of radio signals; later, this theory found extensive application in television transmitters. A phase-locked loop circuit is an up/down converter employed in Radio transmitters and receivers are devices that can create radiation with a frequency range of several gigahertz or higher. It is composed of a series of analog and digital devices that work sequentially to achieve a single goal: to extract a group of high with higher frequencies from a single reference frequency that generates low frequency. (Reddy, 2007).

A Frequency Synthesis Based on a PLL Circuit Because of their great performance and cheap cost, PLL circuits possess numerous uses. Among the many significant uses of PLL circuits includes the ones described below. (Perrott, M. H. (2005).

- A device that can detect low-power signals, such could contain knowledge along with their speed and phase.
- Phase-Locked Loops (PLLs) can be utilized in various applications including clock recovery circuits, tracking systems, demodulators, and frequency multipliers. They are essential for synthesizing precise frequencies, recovering clock and data signals.
- They found usage in space measurements and tracking systems that necessitate signals with high purity and small bandwidths after being created with highly advanced architectures.
- It finds numerous uses in the dual-phase and quadruple-phase domains complicated phase

switches, transmissions splitters, modulator and demodulated signals, and the electromagnetic spectrum

- It is used in the communication field by transmitting and receiving devices for analog controlled AM and FM frequency-modulating circuits.

Methods of frequency synthesis Numerous methods for frequency synthesis are possible. The most commonly used techniques are: first, direct analog synthesis; second, direct digital synthesis; third, indirect synthesis based on a PLL structure (Desikachari, 2003):

1.1. Direct Frequency Synthesizers

Digital frequency synthesizers include digital recollection, a DAC, a sampler, a filter, and a divider, while analog frequencies synthesizers can be made up of a variety of components. A reference clock and a digital memory's signal frequency are same. Converting digital signals into analog ones is the primary function of DACs.

1.1.1. Direct analog frequency synthesizer

Frequency multipliers, dividers, mixers, and band-pass filters (BPF) are used in succession to create stages of a direct analog synthesizer (Jespers, 2001).

1.1.2. Direct digital frequency synthesizer

Direct digital synthesis (DDS) is a digital method used to generate precise and flexible waveforms. Key components of a Direct Digital Frequency Synthesizer (DDFS) include a phase accumulator, a digital-to-analog converter (DAC), a filter, and a phase-to-amplitude converter, often implemented as a sine look-up table. The output sine wave frequency is determined by three factors: binary value input into phase register (frequency control), reference clock frequency, and output from phase accumulator (Shrimali, 2007).

1.2. Indirect Frequency Synthesizers

They generate signals using a PLL configuration. Conventional and digital blocks interact in this most popular form of spectrum synthesizer, which has benefits that make it well-suited for usage in electromagnetic applications. technique achieves a few megahertz with minimal cost and energy consumption in high-frequency programs, together with great precision, rapid settling time, and less phase noise compared to the preceding two methods. Indirect frequency synthesizers based on phase-locked loop technology, such as fractional-N and integer-N PLL frequency synthesizer are among the most important. Indirect frequency synthesizers based on digitally implemented logic loops (DLLs) and two types of equal-spacing phases (Wu et al., 2005).

1.2.1. Frequency Synthesizer in integer -N Phase Locked Loop

A real circuit oscillator (VCO), phase-locked-density (PFD), references input, and a digital

partition with a positive integer division ratio (N) make up an indirect frequency synthesizer technique which incorporates analogy and digital components.as shown in Fig.1.

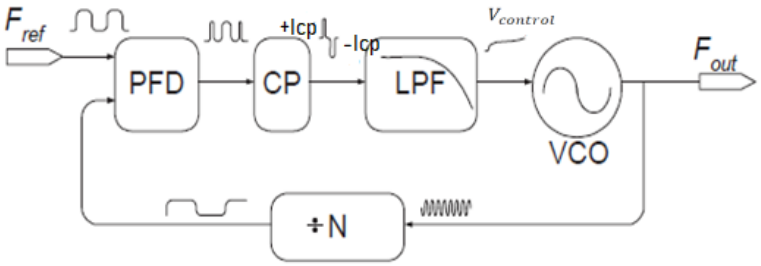

Fig. 1. Integer-N PLL frequency synthesizer circuit

The following is basic method of operation. If control voltage is initially set arbitrarily, VCO first oscillates at its natural frequency. The phase difference between VCO output, φout and reference signal, φin, divided by frequency divider, is compared by PFD.A sequence of pulses with a duty cycle proportionate to phase difference (φin − φout) is PFD's output. The voltage pulses are transformed into current pulses with a preset amplitude I by CP. The loop filter regulates frequency of VCO by converting current pulses into a low-pass filtered voltage signal. In event that feedback is negative, error between φIN and φOUT will progressively decrease until φIN = φOUT. The loop is said to be locked in this state. The frequency of VCO output once loop is locked is equal to frequency of reference times feedback factor N (Rategh and Lee, 2001).

1.2.2. Fractional-N PLL Frequency Synthesizer

Regarding design of circuit components and circuit operation, It employed an inverse fraction division ratio instead of a value that was integer, but otherwise it was identical to integer-N frequency synthesizer. Fig.2 illustrates Fractional –N PLL. Trade-off issue with Integer-N PLL is resolved by Fractional-N PLL, which offers a higher loop bandwidth, more frequency resolution, and less phase noise. Faster switching times are result of greater bandwidth on the loop. Fractional-N PLL has a particular output frequency:

$$Fout = (N.\alpha) * Fref \quad (1) \qquad (1)$$

Where α and N are integers represent fractional component. For calculating the correct fractional division ratio, a dual-modulus divider averages several cycles of integer divider across time (Gu and Ramaswamy, 2007).

Sigma-Delta modulation method and Fractional-N PLL frequency synthesizer (Fatahi and Nabovati, 2010). This system consists of a detector for phase frequency (PFD) In a PLL circuit, it is the very first block. It takes two input signals and generates a sequence of differential square waveforms that are the width of which is dependent to the magnitude of the phase difference.

Next to PFD is a CP, or charge pump. Analog signal, analog-digital signal, and electromagnetic circuits all make use of this component, and in order for them to be noise-proof, they must be housed in a phase-locked loop circuit. There are two ways current can go into the charge pump. Both current sources have connections on the DN end, one is a current sink type which is connected to the PFD's error negative signal, and the other is a VCCS (Voltage Control Oscillator Current Source) type that controls the switching process on the up end. A low-pass filter (LPF) and voltage control oscillator (VCO) are employed to reduce noise from the charge pump current (I_(CP)) before it is sent on to the rest of the circuit. A phase-locked loop circuit in a mixed-signal system is built upon a low pass filter. The main objective of using this piece of equipment is to transmit the low frequencies of the intended signal while eliminating a range of frequencies damage stability. These high frequencies reflect the ac voltage that is a result of the divider's quantization and the nonlinear properties of the circuit elements. Because the loop filter controls the PLL frequency synthesizer's bandwidth and, consequently, its constant working duration, the coefficients of the filter affect the synthesizer's overall performance, comprising open- and closed-loop gains, phase margin, and, most significantly, working duration. importantly, stability.

As the filter order increases, more, the filter transfer function receives its poles, which improves the circuit's output signal by reducing noise. One analog component of a phase-locked loop (PLL) is a voltage-controlled oscillator (VCO), which changes the voltage into a frequency. To rephrase, it serves as a closed-loop negative feedback system that starts by amplifying its own internally generated noise, then feeds that noise back into itself, eventually producing a periodic output signal. A variable-controlled oscillator's (VCO) primary function is to modify the output frequency. The ability to alter output is the most important aspect of a VCO.

An essential and unique element in frequency synthesizer circuits, the frequency division allows for operation at exceedingly high frequencies. Its job is to split the high-frequency output of the VCO to ensure that the PFD may compare it to the benchmark frequency, as shown in equation (2).

$$F_{div} = \frac{F_{out}}{N} \qquad (2)$$

Reducing the extremely high output frequency of the VCO often necessitates the installation of a pre-scaler, which is a collection of divider blocks. For example, in Integer -N PLL frequency electronic instruments the consumer can select their favorite channel by using a configurable move between the various channels of frequency using a multi-bit control signal as a counter, with the division ratio set to a fixed channels frequency. On the other hand, in fractional-N PLL frequency synthesizers, the division proportional is variable and can take on a fractional

number. (Naktal, 2021; Shehab and Yonis, 2024).

To find necessary fractional division ratio, a dual modulus divider is utilized to average numerous integer/divider cycles over time. Using a simple digital accumulator with an overflow controlling dual modulus divider, fractional ratio can be produced. The primary issue with this approach is that fractional spurs, or spurious tones, are produced by dual modulus divider's periodic operation. If first fractional spurs are detected inside loop bandwidth, issue can be resolved by decreasing loop bandwidth in order to eliminate the spurs; however, this will result in an increase in switching time. The spurs are found at (α. Fref). The easiest way to eliminate the fractional spurs without compromising the loop bandwidth is to use a Sigma-Delta modulation technique to break dual modulus operation's periodicity. For the first a period of time Miller and Riley utilized Sigma-Delta Modulator (ξ-Δ) technology, commonly referred to as Delta-Sigma Modulator (DSM), in fractional-N PLL frequency synthesizer circuits as a digital frequency divider control. Because it eliminates the repetitive task of dividing falls somewhere in the middle of two integers, but instead produces a mean value that is equal to the target fractional value, the Σ-Δ modulator has become a vital component of data converters circuits. This is because it produces a signal with high wavelength purity, free from spurious noise that distorts significant data. (Ye et al., 2007; Naktal et al., 2021).

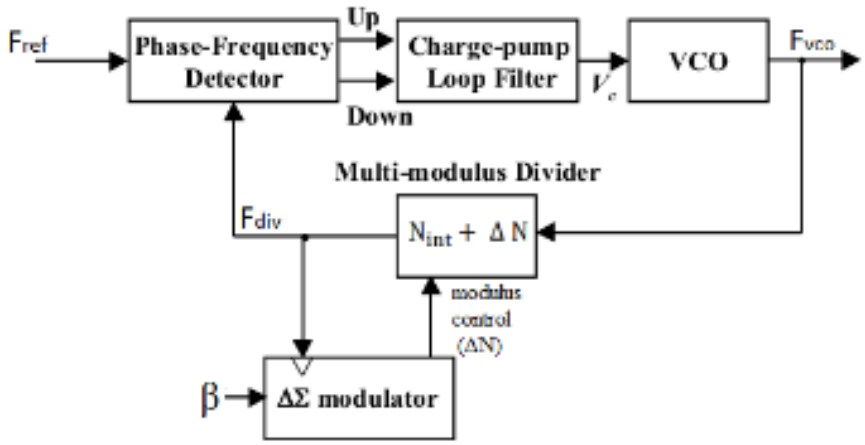

Fig. 2. Sigma-Delta Fractional-N PLL block diagram.

1.3. Aim of Study Through

- Recognizing significance of employing a PLL circuit as a frequency synthesizer in telecommunications, various types of PLL circuits are utilized, each with specific applications and associated challenges.
- To achieve optimal design for Fractional-N PLL circuit, goal is to deliver superior performance for IEEE 802.11 Wireless Local Area Network (WLAN) system. This entails

generating a high-frequency signal characterized by low phase noise, minimal spurious emissions, exceptional recognition of signals precision, and the ability to swiftly transition between several frequency channel.

2. LITERATURE REVIEW

- In 2016, a study focused on creation of an ADS and MATLAB-based fraction frequencies synthesizer. The design implemented a single-loop Sigma-Delta modulator in conjunction with a passive loop filter, evaluated across three different orders to enhance performance of fractional-N Phase-Locked Loop (PLL) in compliance with WLAN standards. The research concluded that optimal configuration consisted of a implementing This fractional-N PLL combines a third-order loop filter with a second-order Sigma-Delta modulator. frequencies synthesizer. This design successfully produced a high-frequency output signal with minimal spurious noise, acceptable phase noise levels, and rapid switching times, achieving -125.5 dBc/Hz at 2 MHz and -131.5 dBc/Hz at 3 MHz.
- In 2019, Heng et al. employed using a combination of IIR (Infinite Impulse Response) and noise phase filtering technique for a Σ-Δ Fractional-N PLL operating at 2.4 GHz. This IIR phase noise filtering approach demonstrated a suppression of phase noise by an additional 5 dB compared to equivalent or lower-order hybrid finite impulse response (FIR) filtering techniques, while occupying a smaller area and achieving lower or comparable power performance. The resulting in-band phase noise was reduced to -102 dBc/Hz at a 100 kHz offset, with fractional spur level measured at -54.7 dBc.

2.1. Wireless LAN Technology (IEEE 802.11)

IEEE 802.11 standard encompasses a broad range of extensions released periodically, with original Wi-Fi standard published in 1997, supporting data rates up to 2 Mbps. This initial standard is now outdated due to continually increasing performance requirements of wireless networks, prompting the development of new techniques and protocols (Hiertz et al, 2010; Abdelrahman et al,2015; Masood 2013; Bellalta 2016). Each subsequent addition to IEEE 802.11 standard, identified by successive letters, introduces enhancements in PHY and/or MAC layers.In parallel, cellular networks play a crucial role in modern communication systems, providing extensive connectivity and efficient data transfer over large distances. Advancements in cellular technology, particularly transition from 4G to 5G, have significantly improved network capacity, data rates, and latency, facilitating a range of new applications. Typically, 5G networks can achieve speeds of up to 10 Gbps. A comparison of wireless network standards is provided in Table1.

Table 1. Comparison Between IEEE 802.11 additional features
(Muhammad et al,2021; Jansen and Kennedy 2020; Sammour 2023; IEEE 2023)

Wi-Fi Standard	Frequency Band	PHY Maximum Data Rate	Modulation Antenna Tech.	Rang m	
				Max. distance	Max. distance
Wi-Fi 1(802.11b)	2.4 GHz in 2.4 GHz ISM	11 Mbps	CCK,DSSS, (SISO)	30-35	120
Wi-Fi 2(802.11a)	5 GHz	54 Mbps	OFDM (SISO)	50	50
Wi-Fi 3(802.11g)	2.4 GHz in 2.4 GHz ISM	54 Mbps	DSSS,OFDM, backward compatible with Wi-Fi 1 SISO	30-70	140
Wi-Fi 4(802.11n)	2.4 GHz &5 GHz	Up to 600Mbps	Higher throughput improvements using MIMO dual-band operation	50-75	250
Wi-Fi 5(802.11ac)	5 GHz	Up to 3.5Gbps	Very High Throughput <6 GHz; potential improvements over 802.11n: MU-MIMO, beamforming, single-band operation	35-70	160
Wi-Fi 6(802.11ax)	2.4 GHz &5 GHz	Up to 9.6Gbps	OFDMA, MU-MIMO, improved MIMO		10
Wi-Fi 7(802.11be)	2.4 GHz &5 GHz	Up to 30Gbps	MU-MIMO, advanced OFDMA, low-latencylatency design		-

CCK: Keying Systems that Work Together: OFDM indicates orthogonal frequency division multiplexing, and DSSS means for direct sequenced spread spectrum. acronyms for "multi-input multiple-output" and "single-input single-output"
Different Users for Different Inputs "Multi-Output," that stands for "multi-user multi,",-

2.2. The Σ-Δ MODULATOR technique THE FRACTIONAL N-PLL CIRCUIT IS DESIGNED AND SIMULATED USING.

This study presents implementation results of Fractional-N Phase-Locked Loop (PLL) circuits utilizing MATLAB 2022b and ADS 2020, designed as a frequency synthesizer for 2.4 GHz bands, compliant with wireless local area network standards (IEEE 802.11a, b, n, ac, ax). A critical aspect of PLL and frequency synthesizer design is loop filter. Key performance metrics, including open-loop and closed-loop gains, phase margin, and overall stability, are essential for effective operation. The target phase margin is typically set between 45° and 60°, with loop bandwidth, comparison frequency, and value of N significantly influencing spurious levels. The design process involves a trade-off between lock time and spurious responses. Notably, optimization of filter components, especially focusing on impact of gamma (γ) parameter on noise performance, was a significant contribution of this work. The γ optimization factor plays a crucial role in loop filter design. Results include a comparative analysis of simulated frequency responses of synthesizer circuits. Additionally, simulation outcomes addressed noise characteristics, encompassing spurious noise, settling time, output spectrum Per circuit's sigma-

delta modulator design was also incorporated into results. This work aims to develop a Fractional-N PLL circuit with specifications tailored for wireless LAN applications. A detailed methodology for determining essential design variables is presented, incorporating fundamental theories and accounting for non-ideal effects such as phase noise and reference spurs.

3. SIMULATION RESULTS AND DISCUSION

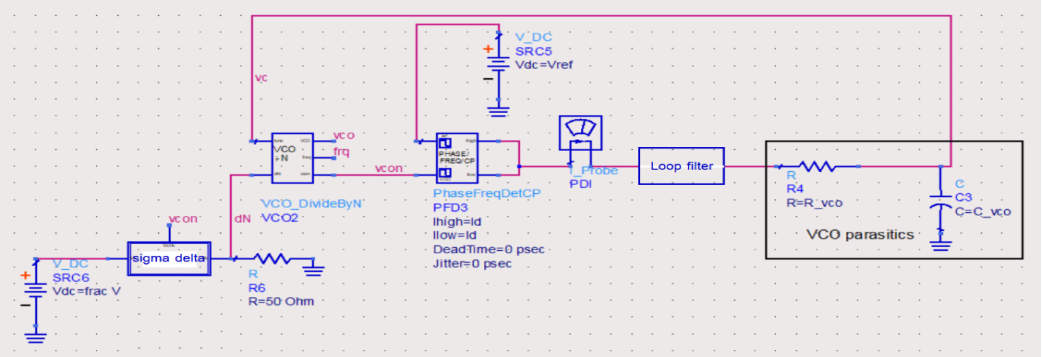

Fig. 3. Structure of Fractional frequency synthesizer circuit.

3.1. Design and simulation of a 2.4 GHz frequency synthesizer for wireless local area networks (WLAN).

3.1.1. Simulation results of 1st proposed frequency synthesizer circuit at pm=575

This section presents and analyzes simulation results for initial design of a Fractional-N PLL circuit featuring a second-order loop filter and a first-order Σ-Δ modulator. The design parameters are as follows in ref (Debnath, S. (2015).: Kvco = 760 MHz, Kϕ = 100 μA, and Fref = 40 MHz. The performance was evaluated across various bandwidths (50, 75, 100, 175, and 250 kHz) and phase margins (48° and 57°). This includes simulations of a sigma-delta modulator of first order using the ADS program, which presents simulation results for divide ration and output spectrum modulator output spectrum and settling time of factional-N PLL circuit.

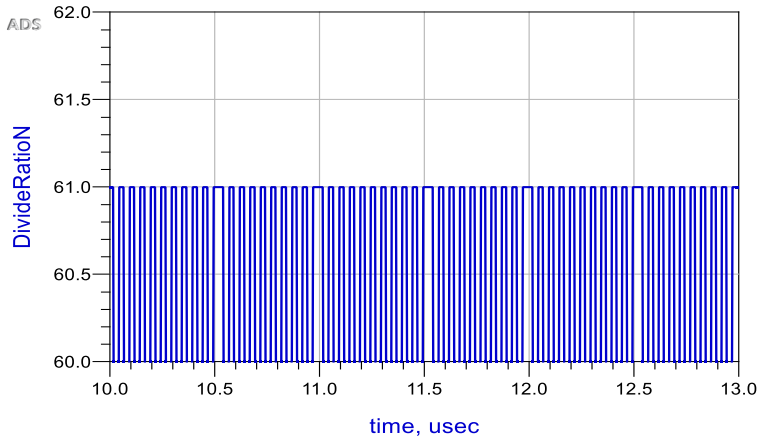

Fig. 4. Total division ratio of 1st proposed frequency synthesizer.

Fig.4 shows that the necessary total division ratio (60.05) is the combination of two consecutive integer values (60) and (61).

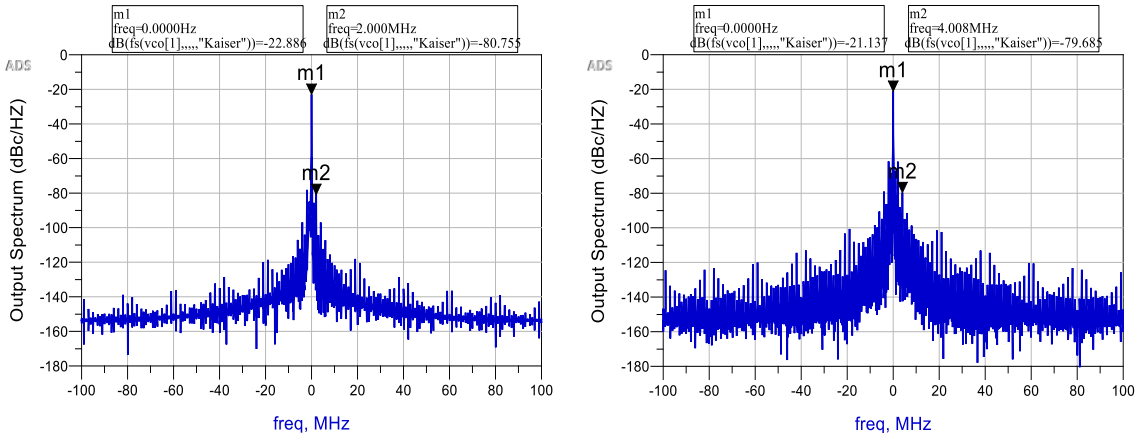

Fig. 5. Output spectrum of 1st proposed frequency synthesizer at BW=125and 50 KHz

The initial harmonic synthesizer circuit that was suggested had a frequency bandwidth of 125 and 50 kHz and produced an output spectrum with a 57° phase margin. The constructed circuit exhibits poor output spectral behavior at bw=125 kHz, as seen in Fig.7a, because it contains high quantities of noise, specifically fractional spurs noise, reference leads noise, and phase noise. The following equation (3) can be used for determining the spurs loudness levels in ref (Banerjee, D. D. (2006).

$$\text{Spurs Level} = P\_Noise_{(at\ offset\ freq)} - P\_Carrier \qquad (3)$$

Where $P\_Noise_{(at\ offset\ freq)}$ represents the magnitude of the noise signal at an exact frequency offset, while P_Carrier stands for the power of the carrier signal. Fig.7 shows that at 2 MHz frequency offsets, the primary level of fractional spur noise (-41.217 dBc) appears, and at 26 MHz frequency offsets, the first level of reference spur noise (-114.833 dBc) appears. utilizing equation (4) in reference, phase noise can also be quantified. (Banerjee, D. D. (2006).

$$\text{Phase Noise (PN)} = (P\_Noise_{(at\ offset\ freq)} - P\_Carrier - 10\ log\ (1.2 * RBW) + 1.05\ dB + 1.45\ dB) \qquad (4)$$

The logarithmic intensity of the noise signal for a Gaussian-type spectrum analyzer is 1.45, the detection response value for a spectrum analyzer is 1.05, and RBW is the bandwidth precision of the instrument's detector. Phase noise for 2 MHz frequency offsets will be -88.659 dBc/Hz. At frequency offsets of 3 MHz, it is equal to -120.871 dBc/Hz. These readings are beyond of the permitted range for 2.4 GHz WLAN IEEE 802.11 standards, which stipulate that the phase noise value must be -110 dBc at 2 MHz bandwidth offsets and -119 dBc at 3 MHz frequency offsets. It is also important to determine how quickly the frequency synthesizers circuit can

shift between channel and how long it takes for the oscillator's output signal to stabilize. At 125 and 50 kHz bandwidth and 57° phase margin, Fig.8 displays the values corresponding to the settling reaction time for the first frequency synthesizer that was proposed. Hence, as shown in Fig.7b, reducing the range of frequencies is one of the techniques used to lower spurious noise and phase noise levels. The output frequency signals has a lower noise level when the bandwidth of the device is reduced to 50 kHz, as shown in Fig.7b, when compared to the prior design of the frequency synthesizer at 125 kHz. At bandwidths of 125 kHz, 100 kHz, 75 kHz, and 50 kHz, all with a 57° phase margin, Table 2 compares for a Fractional N-PLL circuit that uses an a first-order sigma-delta modulation and a the second-order loop filter, the noise power (phase noise, fractional noise, and references noise).

Table 2. Assessment of the first planned frequency synthesizer's noise power at PM= 57°

Bandwidth kHz	Noise Power				
	Phase Noise dBc/Hz		Reference Spurs Noise dBc	Fractional Spurs Noise dBc	
50	-106.160	-141.996	-119.095	-55.264	-74.119
75	-98.208	-130.422	-117.147	-49.588	-67.196
100	-92.885	-124.864	-115.964	-45.152	-62.288
125	-88.659	-120.871	-114.833	-41.287	-58.331
250	-74.114	-107.929	-98.092	-27.561	-45.083

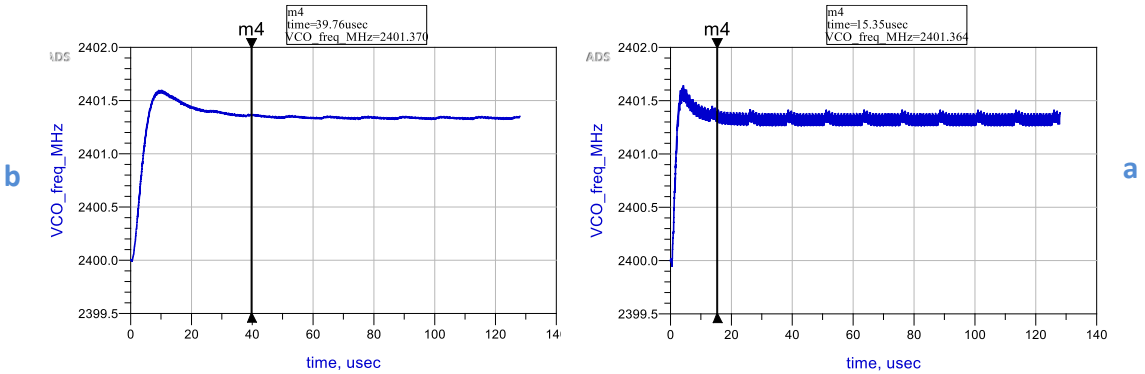

Fig. 6. Output frequency of 1st proposed frequency synthesizer at BW=125and 50 KHz.

The analysis of Fig.7a indicates that designed circuit demonstrates a satisfactory stability time, falling within acceptable range of approximately 15.35 ≤ 220 µs for 2.4 GHz IEEE 802.11 applications. However, circuit exhibits inefficiencies due to elevated levels of spurious noise and phase noise. To address this, the bandwidth of circuit was reduced to 50 kHz of Fig.7b to evaluate impact of bandwidth on spurious noise and phase noise levels within output spectrum of frequency synthesizer. Notably, there is an inverse relationship between bandwidth and settling time; settling time decreases with increasing bandwidth.

3.2. Results of the Second Proposed Frequency Synthesizer Circuit in Simulation

Based on observations from it was discovered that the findings for phase noise, fractional spurs

noise, and reference spurs noise were unsatisfactory in the prior structure of the frequency synthesizers circuit. In order to reduce the values of phase noise, the rank of the filter was raised. and fractional spurs noise. This led to design of a frequency synthesizer circuit termed "Fractional N-PLL Circuit with a Third-Order Loop Filter and a second-Order Sigma-Delta Modulator," or "Second Proposed Frequency Synthesizer Circuit applying the constants and by applying values of constants in ref Debnath, S. (2015) K_{vco}=760MHz/V, K_{ϕ}=100µA, F_{ref}=40MHz at different values of bandwidth (100,75,50) kHz and for each value of phase margin 48°,57° and 65°.

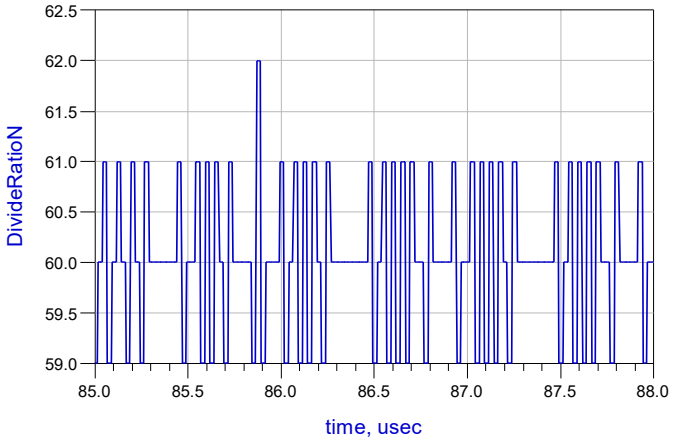

Fig. 7. The second frequency synthesizer being suggested has a total division ratio.

Fig.7 illustrates that output signal from a the second-order sigma-delta the modulator fluctuates among four levels (-1, 0, 1, 2) due to implementation of a two-bit quantize. design incorporates two accumulator circuits that function to push fractional spurious noise to higher frequencies, facilitating its removal by filter and minimizing phase noise at lower frequencies.

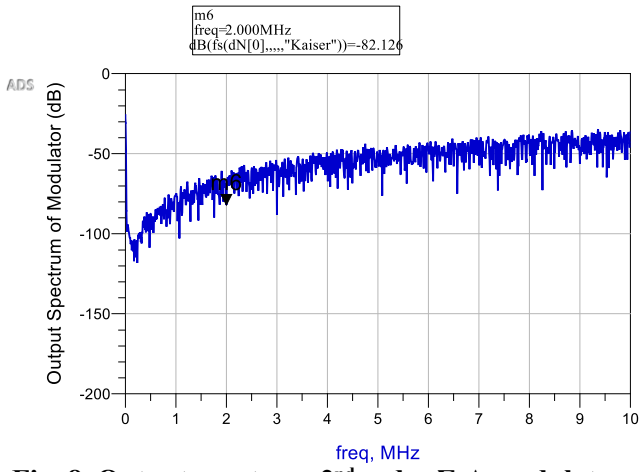

Fig. 8. Output spectrum 2nd order Σ-Δ modulator

Fig.8 illustrates that In contrast concerning the sigma-delta modulation of the initial order, the second-order sigma-delta synthesizer produces a more effective output spectrum. Second-order design is free from fractional spur noise and demonstrates significantly lower noise power levels.

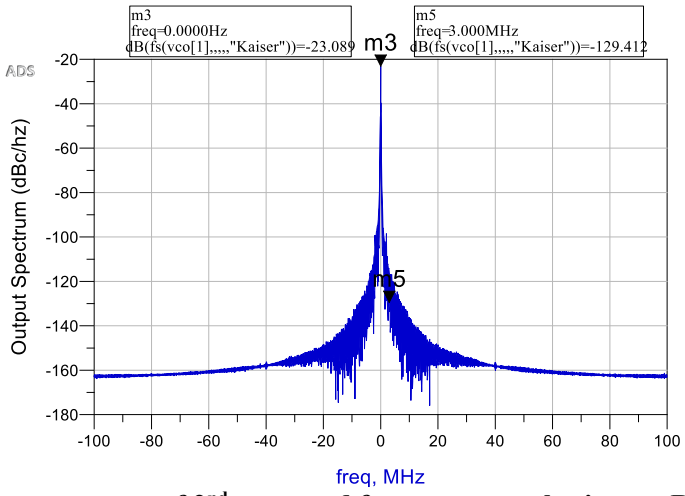

Fig. 9. Output spectrum of 2nd proposed frequency synthesizer at BW=75 KHz

Fig.9 shows that output spectrum of designed frequency synthesizer circuit is free from spurious noise (both fractional and reference) due to noise reshaping properties of quantizer in sigma-delta modulator. Additionally, phase noise has been significantly improved, reaching acceptable levels for WLAN standards, attributed to added pole of third-order filter (T3), which enhances phase noise performance at higher frequencies. Phase noise for designed circuit is measured at -140.118 dBc/Hz at a 2 MHz frequency offset and -154.614 dBc/Hz at a 3 MHz offset in frequency. exhibited phase noise values of -106.160 dBc/Hz at a 2 MHz frequency offset and -141.996 dBc/Hz at a 3 MHz frequency offset, both measured under same bandwidth and phase margin conditions.

3.3. Simulation results of 3rd proposed frequency synthesizer circuit at pm=575

Featuring a third-order sigma-delta modulation and a fourth-order loop filter, this section includes simulation findings as well as comments for Design of circuits number three for frequency synthesizers: the fractional-N PLL devices.

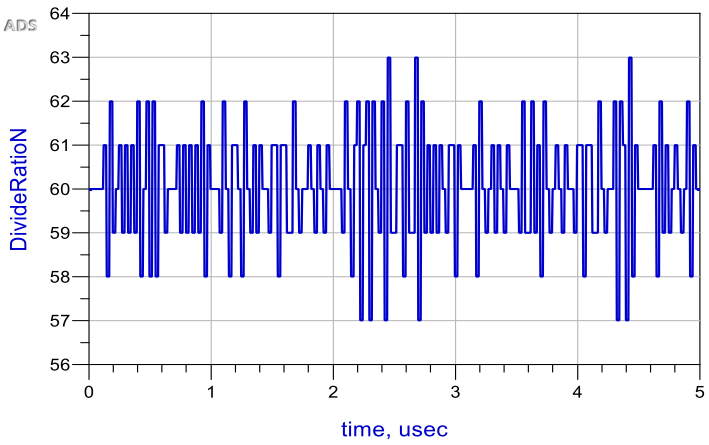

Fig. 10. Ratio of the third frequency synthesizer suggested

Fig.10 shows that output signal of third-order sigma-delta modulator exhibits rapid and random fluctuations to achieve the desired partition ratio, attributed to presence of a multi-bit quantizer.

Additionally, three accumulator circuits are employed to push the fractional spur noise to higher frequencies, enabling its removal by filter and reducing phase noise at lower frequencies. Output spectrum is illustrated in Fig.11.

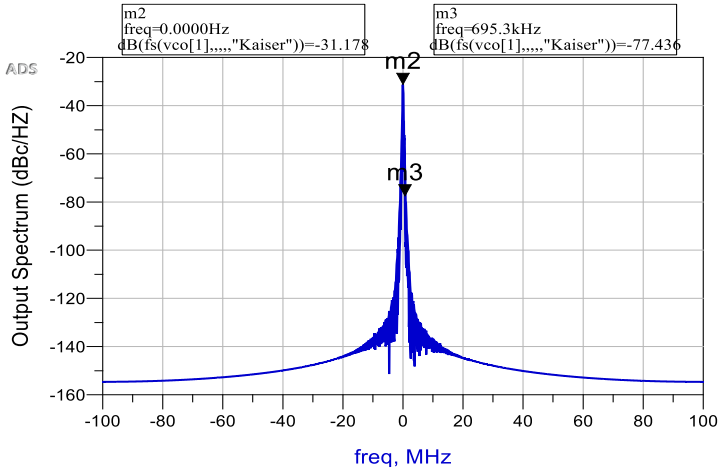

Fig. 11. Output spectrum of 3rd suggested frequency synthesizer to be located at BW=75 KHZ

Fig.11 illustrates that output spectrum of the third frequency synthesizer circuit that has been proposed is free from spur noise, both fractional and reference. This is attributed to the noise reshaping capabilities of quantizer in sigma-delta modulator. However, it is notable that phase noise values at higher frequencies are greater than those observed in previous designs. Specifically, noise value at 2 MHz is -136.591 dBc/Hz, while at 3 MHz, it is -141.849 dBc/Hz, Therefore, we observe that previous design offers improved performance, providing lower phase noise levels, reduced spur noise, and shorter settling times.

4. CONCLUSIONS

This research primarily aims study is to demonstrate a 2.4 GHz Fractional N-PLL design circuit that can generate a pure a high-frequency signal with sufficient precision and speed while conveying it across frequency channels. The impact of the Sigma-Delta (Σ-Δ) modulator on the performance of a Fractional-N Phase-Locked Loop (PLL) was investigated, with different low-pass filter designs evaluated to identify the most suitable configuration that meets IEEE 802.11 standards.

The results indicate that increasing order of Σ-Δ modulator affects performance by:

- Eliminating fractional and reference spurious noise from output frequency signal of synthesizer.
- Reducing phase noise at lower frequencies while increasing it at higher frequencies, as modulator functions as a high-pass filter. Consequently, a higher-order modulator enhances phase noise performance at lower frequencies.

Effect of Filter on Frequency Synthesizer Performance: The performance of frequency synthesizer circuit is influenced by filter parameters (bandwidth, phase margin, filter order):

- Increasing filter order improves phase noise performance at high frequencies. The additional pole of filter helps frequency response approach an ideal state for noise removal in stopband region.
- An increased phase margin enhances both accuracy of output signal and stability time of frequency synthesizer circuit.
- While increasing bandwidth reduces settling time due to its inverse relationship, decreasing bandwidth improves levels of reference and fractional spurious noise in output frequency signal of frequency synthesizer circuit.

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