

Frequency Dependent Capacitance –Voltage and Current Density Characteristic of Al/PS/p-Si Heterojunction

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Abstract

In this paper, formation of microstructures porous silicon layer (PS) on c-Si substrate p-type with resistivity's $10 \Omega.cm$ which was prepared by the electrochemical etching (ECE) is presented. The etching current densities (40 and $50 mA.cm^{-2}$) were used in the electrochemical etching procedure leading to the formation of $1.08 \mu m$ and $1.34 \mu m$ thick porous layers respectively at constant etching time $300sec$. From the current – voltage characteristics of the PS/p-Si, the potential barrier were determined and found to be (0.54 and $0.53 eV$) respectively. C-V measurements performed on metal/porous silicon/crystalline silicon structures with different etching current densities and frequency depended.

Keywords: Nano-structure, Porous Silicon, Electrochemical Etching (ECE) and Heterojunction.

إعتماد التردد على خصائص السعة – فولتية وكثافة التيار للمفروق الهجين Al/PS/p-Si

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الخلاصة

في هذا البحث تم تشكيل التركيب المايكروني لطبقة السيليكون المسامي (PS) على القاعدة السيليكونية من النوع الموجب ذي المقاومة $10 \Omega.cm$ المحضر بطريقة التتميش الكهروكيميائية . ان قيم كثافات تيار التتميش في الطريقة المستخدمة للحصول على سمكي طبقة السيليكون المسامي $1.08 \mu m$ و $1.34 \mu m$ هي على التوالي ($40 mA.cm^{-2}$ و $50 mA.cm^{-2}$) بثبات زمن التتميش عند القيمة 300 ثانية. من خصائص تيار –فولتية للتركيب PS/p-Si تم حساب قيمة حاجز الجهد والذين هما $0.54 eV$ و $0.53 eV$ لكلا التركيبين على التوالي. دراسة خصائص السعة – فولتية لتركيب المعدن/ السيليكون المسامي/السيليكون البلوري والتي اعتمدت على كل من كثافة تيار التتميش والتردد.

الكلمات المفتاحية: تركيب نانوي ، السيليكون المسامي ، التتميش الكهروكيميائي و المفروق الهجين

Introduction

Porous material has been a subject of investigation for many years, since it offers many attractive features such as light weight, large surface-to-volume ratios, low dielectric constant and low thermal conductivity (Rihui, *et al.*, 2004), Anaheim, California USA. Porous silicon PS is a network of air holes in a silicon matrix. Porous silicon has a merit that it can be easily prepared by the simple electrochemical anodization of silicon (Hong, *et al.*, 2011). Few types of anodization cells for the fabrication of PS have been used thus far. Conventional cells such as a single-tank cell, Al after both the Si wafer and the Pt counter electrode are entirely immersed into hydrofluoric (HF) solution (Park, *et al.*, 2010). It is well-known that the interface properties have a dominant influence in the device performance, reliability and stability (Temircl, *et al.*, 2001). The barrier height is commonly calculated from the saturation current I_s determined by an extrapolation of the $\log(I)$ versus V curve to $V = 0$. Series resistance is not important in this extrapolation because the current saturation current I_s is very low. The barrier height (ϕ_B) is calculated from the I_s . Capacitance-voltage measurement is one of the most important methods for obtaining information about the rectifying junctions, built-in potential, and junction capacitance and junction type. The excess capacitance is due to traps at the junction interface. These traps can be created by dangling bonds, inter-diffusion of atoms and crystal defects at the metal/semiconductor (Ahmad, *et al.*, 2011). As a negative voltage is applied, the potential across the semiconductor increases and so does the depletion layer width. As a positive voltage is applied, the potential across the semiconductor decreases along with the depletion layer width. The total potential across the semiconductor equals the built-in potential minus the applied voltage. The built-in potential in

a semiconductor equals the potential across the depletion region in thermal equilibrium (Ahmad, *et al.*, 2011 and Farag, *et al.*, 2009). In this paper, the metal/porous silicon layer /silicon formed by electrochemical etching of p-Si. The characteristic parameter obtained from the current –voltage (I-V) and capacitance –voltage (C-V) characteristics of the structure Al/PS/p-Si/Al.

Materials and Methods

Porous silicon samples were prepared by electrochemical etching of p-type Si (111) plates with resistivity's $10 \Omega \cdot \text{cm}$. Solution of 40% HF in methanol 99.8% in proportions HF: CH_3OH as 1:1 was used as etchant at room temperature. Porous silicon layers were produced using monocrystalline silicon wafers. The porous silicon PS samples were obtained at values of current density J of 40 and 50 mA/cm^2 and etching time T of 300 sec. The thickness of porous layer were 1.08 μm and 1.34 μm at of 40 and 50 mA/cm^2 respectively at constant etching time 300sec by using theoretical relation (Hadi, *et al.*, 2013):

$$d = R J^x T \dots\dots\dots 1$$

Where d is the layer thickness, $R = 0.0000105$, $x = 0.96$ and T etching time. The etched crystalline silicon was (111) oriented wafer, p-type with resistivity's $10 \Omega \cdot \text{cm}$. Porous silicon layers were produced using monocrystalline silicon wafers. The porous silicon (PS) layers were prepared by anodic etching using an electrolyte containing 40% solution of HF and methanol (1:1) at room temperature. The etching current densities (40 $\text{mA} \cdot \text{cm}^{-2}$ and 50 $\text{mA} \cdot \text{cm}^{-2}$) were used in the electrochemical etching procedure leading to the formation of 1.08 μm and 1.34 μm thick porous layers respectively at constant etching time 300sec by using theoretical relation 1. The samples are prepared in sandwich configuration, top Al/PS/c-Si/bottom Al, the top one electrode thermally evaporated with thin layer and the bottom electrode is coated with thick Aluminum layer before the

anodization process as shown in figure (1).

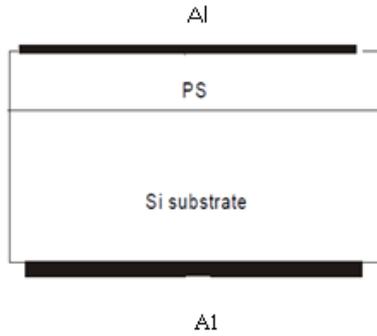


Figure (1) Structure with Porous Silicon Layer for (I-V) and (C-V) Measurements.

Dark current – voltage in forward and reverse directions Al/PS/c-Si/Al measurements are carried out by applying voltage supplied to the sample from a stabilized d. c. Power supply, type LONG WEI DC PS-305D 30 ranges (-10 to+10) V. The current passing through the device is measured using a UNI-T UT61E Digital Multimeters. Capacitance - Voltage characteristics of the Al/PS/c-Si HJ heterojunction are measured using a LCR meter at room temperature. The C-V measurements at different voltage bias and frequencies .The barrier height is commonly calculated from the saturation current I_s determined by an extrapolation of the log (I) versus V curve to $V = 0$. During capacity measurements, the voltage between the two contacts was scanned of range (-1.2 to +1.2 V) and we had scanned the frequency range from 20 kHz to 200 kHz.

Results and Discussion

Thickness data showed low effect differences between 40mA/cm^2 and 50mA/cm^2 current densities on thickness layer at constant etching time. Therefore, the layer thickness is related with anodization duration. The formation of the pores and porosity are strongly related with the current-voltage characteristics of the sample and that agree with (Milani, *et al.*, 2006). The increasing of the thickness increases the dynamic resistance of the junction. This can be explained as the smaller current densities pass within the porous

structure although the PS layer has higher dynamic resistance compared with those for low dynamic resistance PS layer as shown in the behavior of (I-V) characteristic in Figures 2 and 3. From these figures (2 and 3) the range of forward dark current at 40mA/cm^2 etching current density reach to $750\text{ }\mu\text{A}$ while at 50mA/cm^2 etching current density was closed to $200\text{ }\mu\text{A}$.

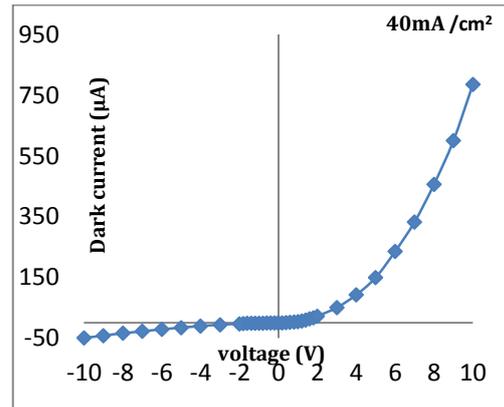


Figure (2) Dark I – V Characteristic of Heterojunction at 40mA/cm^2 .

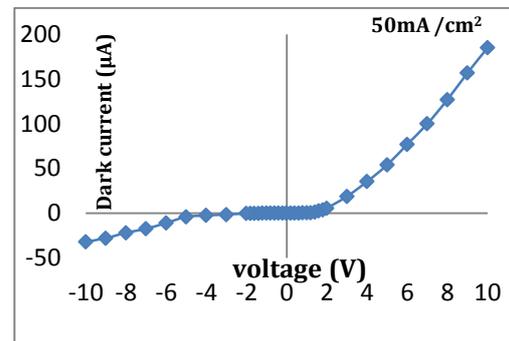


Figure (3) Dark I – V Characteristic of Heterojunction at 50mA/cm^2 .

We can directly calculate from dark forward current, which is carried out at different forward bias voltage at room temperature and plotted in semi-log graphs as shown in figures 4 and 5. The reverse saturation current (I_s) is determined by interpolation of exponential slope of (I) at $V=0$. We measure saturation current density directly from dark forward current, which is carried out at different forward bias voltage at room temperature and

plotted in semi-log graphs as shown in figures 4 and 5 at 40 mA/cm² and 50 mA/cm² etching current density respectively.

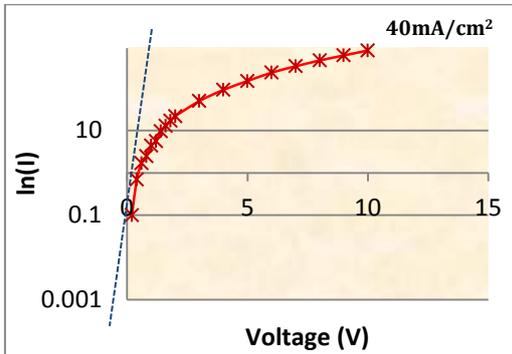


Figure (4) ln (Forward Dark Current I_D) Versus Bias Voltage

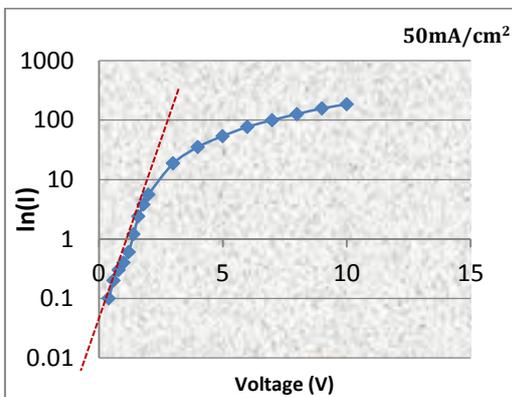


Figure (5) ln (Forward Dark Current I_D) Versus Bias Voltage.

The barrier height is commonly calculated from the saturation current I_s that determined by an extrapolation of the $\ln(I)$ versus V curve to $V = 0$. Series resistance is not important in this extrapolation because the current I_s is very low. The barrier height ϕ_B is calculated from I_s in the next Eq. (Milani, *et al.*, 2006):

$$I_s = AA^*T^2 e^{-\frac{q\phi_B}{KT}}$$

$$= I_{s1} e^{-q\phi_B/KT} \dots \dots \dots 2$$

where A is the diode area, $A^* = 4\pi qk^2m^*/h^3 = 120 (m^*/m) A/cm^2K^2$ is Richardson's constant⁴, ϕ_B the effective barrier height, Equation 2 is sometimes expressed as:

$$\phi_B = \frac{kT}{q} \ln\left(\frac{AA^*T^2}{I_s}\right) \dots \dots \dots 3$$

The barrier height so determined is ϕ_B at zero bias. The most uncertain of the parameters in Eq. 3 is A^* , rendering this method only as accurate as A^* is known. Fortunately, appears in the "ln" term. For example, an error of two in A^* gives rise to an error of $0.69 kT/q$ in ϕ_B (Milani, *et al.*, 2006).

From the current – voltage characteristics of the PS/p-Si, the potential barrier was determined (0.54 and 0.53 eV) respectively. Figures (5-11) show the (C–V and C²-V) measurements of the PS/p-Si heterojunction in dark at room temperature and at the increment voltage of frequencies (20-200 KHz) at 40 and 50 mA/cm² respectively. These results show that the junction capacitance is inversely proportional to the bias voltage for the most of the prepared samples. The C-V characteristics of the prepared device depend on the morphology and the porosity of the etched Si surface since it depends on etching current density, and this in agreement with previous studies (Schroder, 2006). Clearly a show that the external voltage (V) applied across the structure is redistributed among each of the layers, hence. The total capacitance of the structure being considered comprises the two capacities connected in series. Equivalent capacitance was plotted with frequency and it was found that the values are increasing with the frequency range we have used as shown in figures (6-17). The reduction in the junction capacitance with increasing the bias voltage results from the expansion of depletion layer with the built-in potential. The width of the depletion layer the W_D of the porous layer depends on concentration (N_D), and the built-in potential (V_{bi}) is according to equation 3. Therefore, any change in the concentration N_D will change the depletion layer width. As the etching

current increases the pore size increases as well as the depletion layer width, thickness and resistance. With built in voltage V_{bi} , a depletion width should follow a relationship such as:-

$$W = \left[\frac{2\epsilon_i \epsilon_o}{qN_d} (V_{bi} - V) \right]^{0.5} \dots\dots\dots 4$$

$$W = \sqrt{\frac{2\epsilon V_{bi}}{qN_e}} \dots\dots\dots 5$$

where W is related to the junction capacitance C as $W = \epsilon A/C$ where ϵ is permittivity and A is junction area, thus $d = \epsilon_{PS} A / C_{PS}$ where ϵ_{PS} and C_{PS} are permittivity and junction capacitance of PS. The capacitance – voltage characteristics of PS/p-Si structure depend on the morphology and the porosity of the etched silicon surface, where N_D , is the donor density, ϵ_i is the relative permittivity of interfacial layer and ϵ_o is the permittivity of vacuum (Parlakturk, *et al.*, 2007).

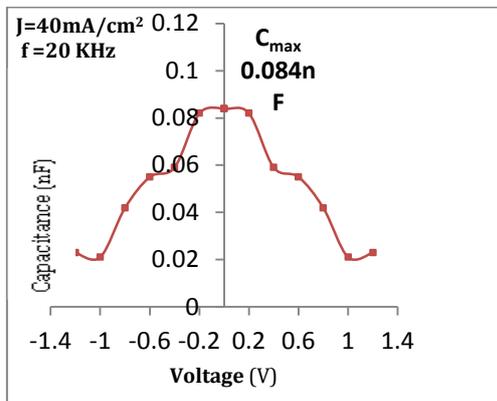


Figure (6) Measured Capacitance(C) vs. Gate Bias (V) for Al/PS/p-Si HJ at 20 KHz Frequency.

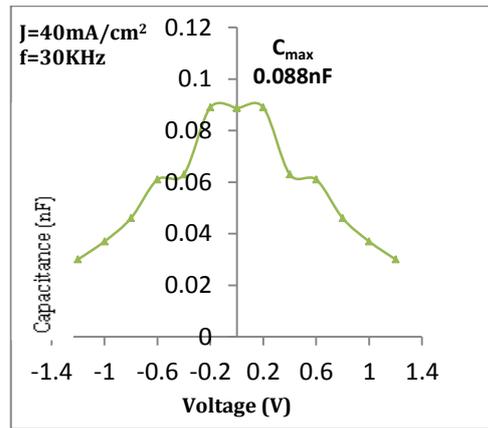


Figure (7) Measured Capacitance(C) vs. Gate Bias (V) for Al/PS/p-Si HJ at 30 KHz Frequency.

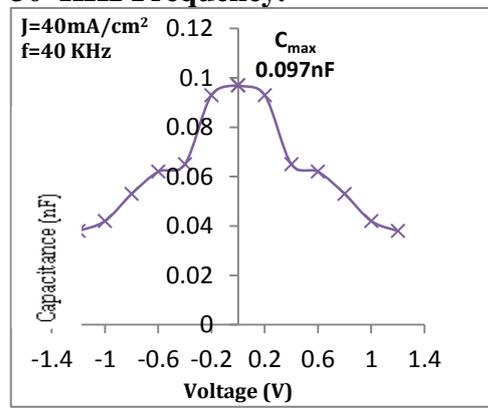


Figure (8) Measured Capacitance(C) vs. Gate Bias (V) for Al/PS/p-Si HJ at 40 KHz Frequency.

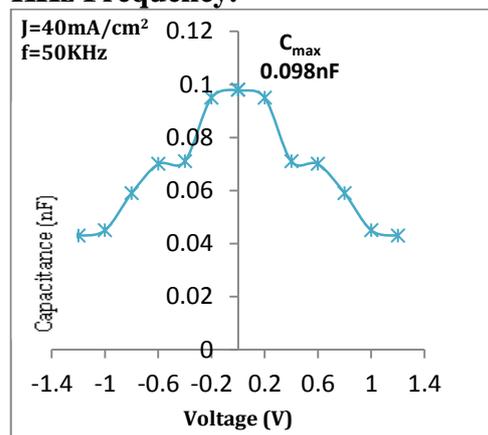
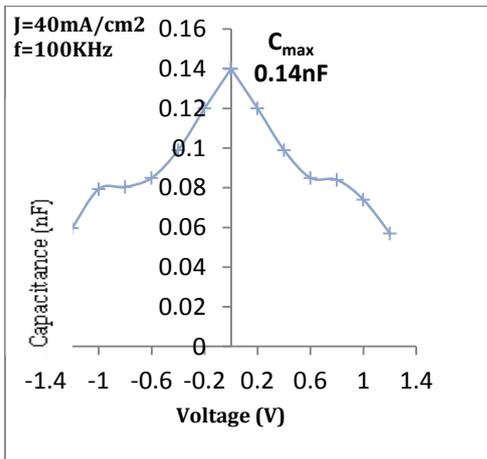
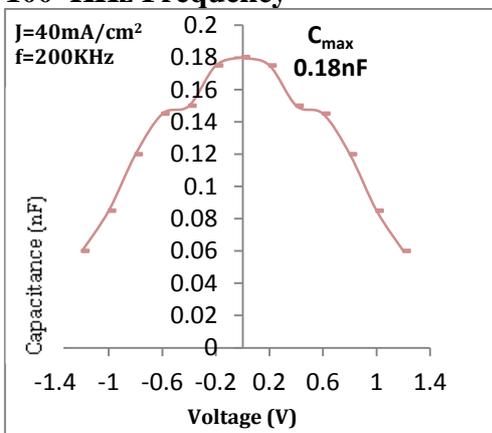


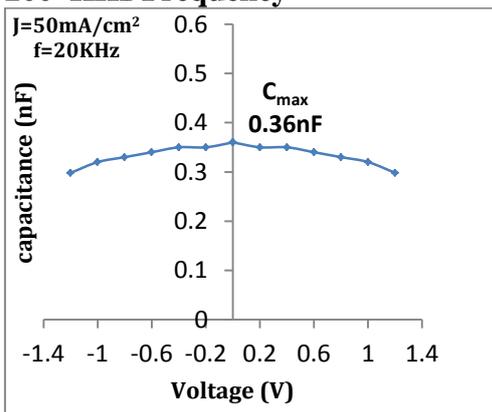
Figure (9) Measured Capacitance(C) vs. Gate Bias (V) for Al/PS/p-Si HJ at 50 KHz Frequency.



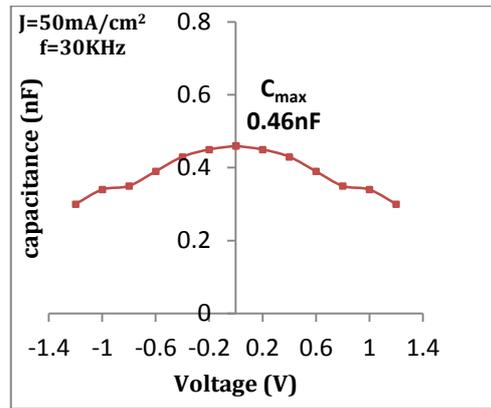
Figure(10) Measured Capacitance(C) vs. Gate Bias (V) for Al/PS/p-Si HJ at 100 KHz Frequency



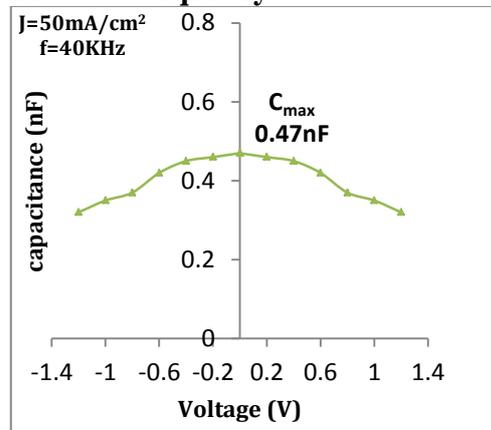
Figure(11) Measured Capacitance(C) vs. Gate Bias (V) Al/PS/p-Si HJ at 200 KHz Frequency



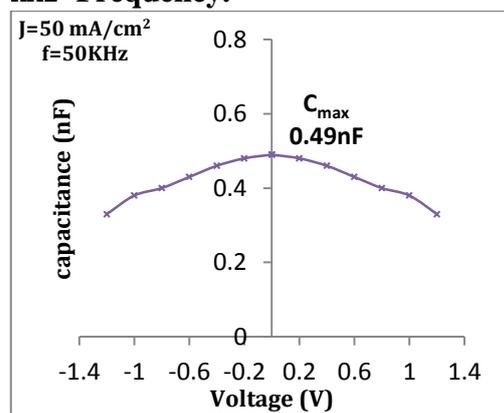
Figure(12) Measured Capacitance(C) vs. Gate Bias (V) Al/PS/p-Si HJ at 20 KHz Frequency



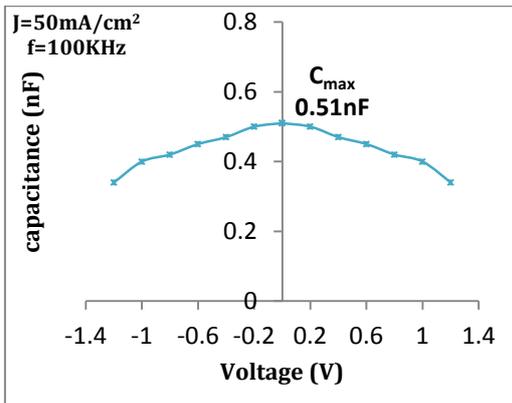
Figure(13) Measured Capacitance(C) vs. Gate Bias (V) for Al/PS/p-Si HJ at 30 KHz Frequency.



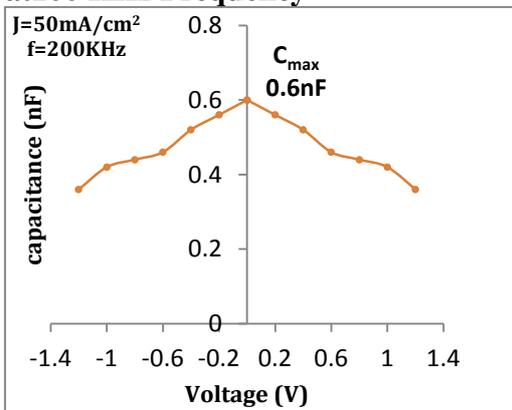
Figure(14) Measured Capacitance (C) vs. Gate Bias (V) Al/PS/p-Si HJ at 40 KHz Frequency.



Figure(15) Measured Capacitance(C) vs. Gate bias (V) Al/PS/p-Si HJ at 50 KHz Frequency



Figure(16) Measured Capacitance(C) vs. gate bias (V) for Al/PS/p-Si HJ at 100 KHz Frequency



Figure(17) Measured Capacitance(C) vs. Gate Bias (V) for Al/PS/p-Si HJ at 200 KHz Frequency.

The value of capacitance increases with the increase in etching current density and the same behavior with increase frequency .this may be due to the time dependent response of interface states. Figures (18 and 19) demonstrate the reciprocal capacitance square C^{-2} versus V does not give a straight line. This means that the depletion layer and the barrier height are not constant and so the carrier concentration will not be constant at the depletion layer.

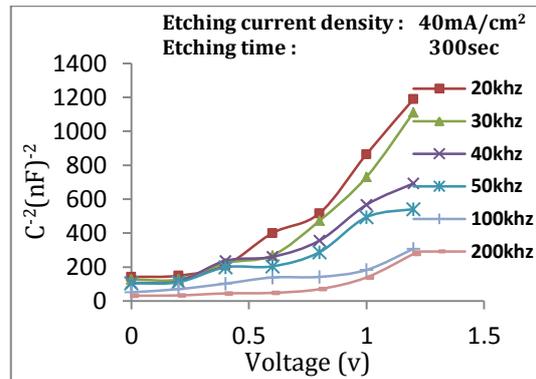


Figure (18) Plot of $1/C^2$ vs V for Al/PS/p-Si HJ Structure at Different Frequency ($40\text{mA}/\text{cm}^2$ Etching Current Density).

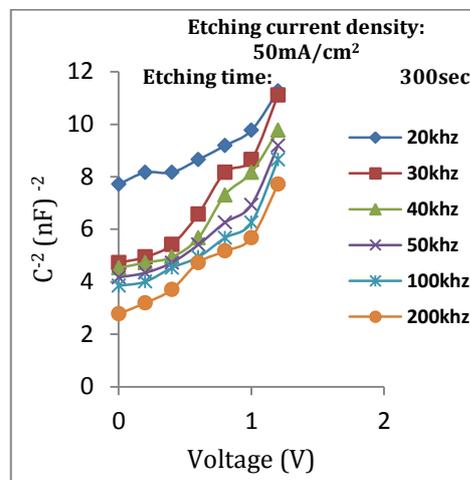


Figure (19) Plot of $1/C^2$ vs V for Al/PS/p-Si HJ Structure at Different Frequency ($50\text{mA}/\text{cm}^2$ Etching Current Density).

Conclusions

The electrical properties of the heterojunction fabricated by electrochemical etching have been investigated. It is observed that the capacitance of heterojunction is very sensitive to frequency and current density. The experimental results showed that the height dependence on the porous silicon preparation condition.

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