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INVESTIGATION AND DEVELOPMENT OF A MULTILEVEL INVERTER WITH A 29-LEVEL REDUCED SWITCH COUNT

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ABSTRACT

A novel multilevel inverter design for electric vehicle applications is presented in this research. In order to generate the necessary twenty-nine levels of output voltage and current waveforms, this multilevel inverter is developed using ten power switches and four distinct asymmetrical DC sources. Pulse width modulation is the most often utilized control method in multilevel inverters. This multilevel inverter uses sinusoidal pulse width modulation to remove low order

harmonics. MATLAB is used for simulation, and a resistive load and resistive-inductive load is used for testing. A 210V, single phase, 29 level proposed architectural prototype uses MOSFETs as switching devices. In the hardware configuration, IRF840 MOSFETs are used. For inverter switches, the Ardiuno micro controller generates the gate signal. To achieve a twenty-nine level output waveform, typical multi-level inverters require a greater number of power components, which raises switching losses, costs, and harmonic distortion. By using 10 switches, the suggested inverter greatly reduces switching losses, low order harmonics, and switching costs, which in turn lowers overall harmonic distortions.

KEYWORDS

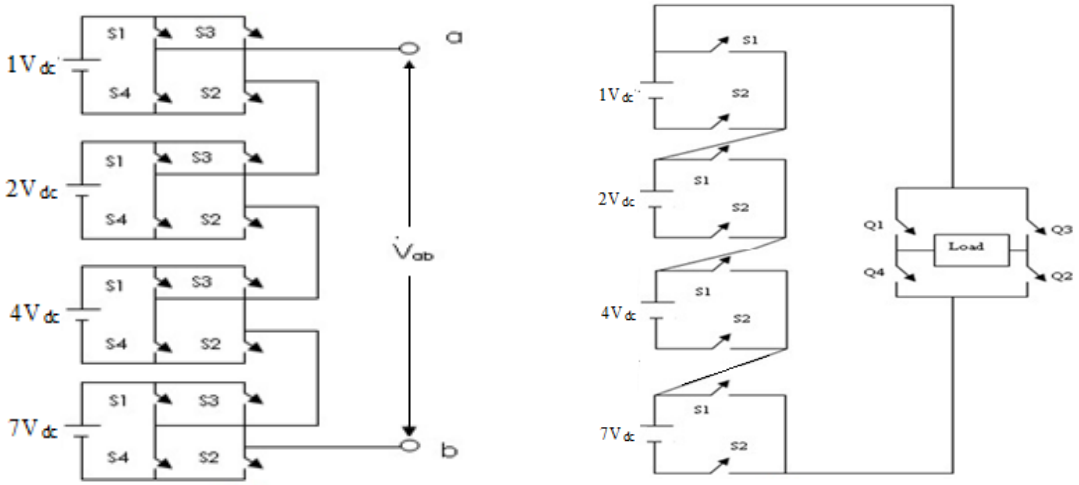
Multilevel Inverter (MLI), Direct Current (DC), Total Harmonic Distortion (THD), Pulse Width Modulation (PWM).

1. INTRODUCTION

Numerous power applications, such as electric cars, solar systems, low-power loads, and grid integration systems (Ravanan et al., 2022; Anssari and Othman, 2019), now make extensive use of multilevel inverters (MLI) (Rodriguez et al., 2001). It's very low harmonic distortion, short installation footprint, switching losses, minimal number of drivers, lack of filters, and reduced voltage stress make it more attractive (Rodriguez et al., 2010). A new single-DC source MLI inverter is available for low power applications. Flying capacitor, diode clamped or neutral point clamped, and cascaded H-Bridge topologies are the general categories of MLIs. Cascaded multilayer inverters have been employed in hybrid systems in recent years (Amirreza et al., 2021). Examining several MLI setups in terms of switching device count and modulation techniques, the recommended inverter's output voltage is eight times higher than the input voltage (Abdul et al., 2021). Staircase voltages may be constructed using a variety of topologies that need fewer devices for greater levels. It has been observed that the harmonic content of the load voltage and current waveforms reduces with an increase in the voltage or current output levels (Tolbert et al., 1998). For the suggested inverter, the total harmonic distortion for resistive and resist-inductive loads is investigated. Diodes and capacitors are employed in the inverter circuits, and a variety of symmetrical, asymmetrical, and hybrid MLI topologies were developed with varying numbers of switches (Tolbert et al., 1999). Additionally, a study of each setup's total standing voltages and THD production is conducted. The number of switches, voltage imbalance, and number of DC sources are among the few shortcomings of all topologies (Corzine et al., 2004). Modern multilayer inverters with fewer switches are primarily focused on higher voltage levels. Higher voltage levels can be achieved by using separated DC voltage sources and cascaded H bridge MLI. The main unit's design serves as the foundation for power component reduction (Fracchia et al., 1992; Corzine and Baker, 2002). Several pulse width modulation (PWM) methods were examined using the decreased switch count structure (Barzegarkhoo et al., 2022). There are now two new MLI structures that are linked to the PV system (Peng, 2004; Manjrekar et al., 2000). Nine output levels are produced by both MLI architectures, which have the same number of power switches (Chiasson et al., 2003).

The setup of traditional multi-level inverters is shown in Fig. 1. To generate 29 levels, each cell needs four independent DC asymmetrical voltage sources ($1V_{dc}$, $2V_{dc}$, $4V_{dc}$, and $7V_{dc}$) linked in series. Sixteen power components in the first arrangement provide twenty-nine output voltage or current levels. In this construction, four H-bridges are involved (Amirreza et al., 2021; Tolbert et al., 1998; Manjrekar et al., 2000). The identical twenty-nine-stage output is produced by the second design using twelve components. Each of the four cells in this

arrangement has two power switches and an asymmetrical DC source, resulting in a multi-stage unidirectional output. Before connecting to the load, an H-bridge circuit is utilized to create a positive and negative half-cycle waveform in the output (Peng, 2004). The need of additional power switches is the main issue with these cascaded MLIs.



Cascaded H-bridge Hybrid MLI New Cascaded Hybrid MLI

Fig. 1. Topology of four H-bridges

Eighteen switch MLI has been presented with the involvement of four capacitors and 18 separate switches (Barzegarkhoo et al., 2022). Thirty-one level MLI is explained with the help of 12 switches, 4 capacitors, and 3 separate DC sources (Dhanamjayulu et al., 2020). Thirty-one level MLI is presented with the help of 16 switches, 2 diodes, 4 capacitors and 2 separate DC sources (Meraj et al., 2019). 31 level MLI is constructed with 10 switches and 4 separate sources (Hamidi et al., 2020). From the literature, it is found that Total harmonics distortion, total standing voltage, cost functions are important factors for the multilevel inverters.

A novel MLI is proposed with only ten power components to generate 29 output voltage or current levels. This construction drastically reduces overall harmonic distortion by 29 levels by using the sinusoidal PWM approach. It provides outstanding output voltage quality with low THD, low TSV per unit, low CF per level that is appropriate for EVs while lowering cost, weight, and complexity.

2. PROPOSED SYSTEM

The assemblage of the projected multi-level inverter is depicted in Fig. 2. There are four asymmetrical DC voltages sources which are linked to ten switches (4 bi-directional-S1, S3, S4, S6, 6 uni-directional) for producing 29-level output.

The number of DC sources required can be calculated by using the following equation,

$$N_{DC} = \frac{N_{Level}}{9} + 1 \quad (1)$$

The number of levels with respect to DC sources can be calculated by using the equation,

$$N_{Level} = \frac{3^{N_{DC}}}{3} \quad (2)$$

The number of diodes required with respect to DC sources can be calculated by using the equation,

$$N_{diode} = \frac{N_{DC}}{2} \quad (3)$$

Various operating modes of proposed MLI is explained,

Mode 1: Switches S4, S5 & S6 conduct and gives zero output voltage.

Mode 2: Switches S2, S3 & S4 conduct and produces $1V_{dc}$=15V.

Mode 3: Switches S2, S3, S4 & S7 conduct and produces $2V_{dc}$=30V.

Mode 4: Switches S2, S3, S4, & S8 conduct and produces $1V_{dc}+2V_{dc}=3V_{dc}$ =45V it supplies to the load.

Mode 5: Here, switches S1, S2, S6 and S10 conduct and produces $4V_{dc}$=60V, it supplies to the load.

Mode 6: Switch S2, S4, S6 and S10 conduct and produces $4V_{dc}+1V_{dc}$ =$5V_{dc}$=75V, it supplies to the load.

Mode 7: Switch S2, S4, S6, S7 and S10 conduct and produces $4V_{dc}+2V_{dc}=6V_{dc}$=90V.

Mode 8: S1, S2 and S6 conduct and load voltage is $7V_{dc}$=105V.

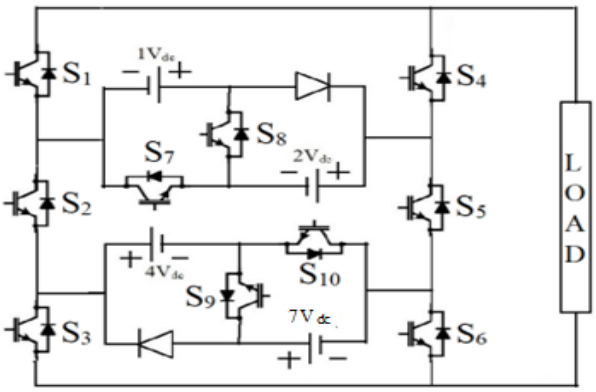


Fig. 2. Proposed Multilevel Inverter

Mode 9: Switches S2, S4 and S6 conduct and now the output voltage is $7V_{dc}+1V_{dc}=8V_{dc}$=120V.

Mode 10: Devices S2, S4, S6 and S7 conduct and now the output voltage is $7V_{dc}+2V_{dc}$ =$9V_{dc}$=135V, supplies to the load.

Mode 11: Switches S2, S4, S6 and S8 conduct and load voltage is $7V_{dc}+2V_{dc}+1V_{dc}=10V_{dc}$=150V.

Mode 12: Switches S1, S2, S6 and S9 conduct and the output is $7V_{dc}+4V_{dc}=11V_{dc}$=165V.

Mode 13: Switches S2, S4, S6 and S9 conduct and output is $7V_{dc}+4V_{dc}$+1Vdc =$12V_{dc}$=180V across the load.

Mode 14: Switches S2, S4, S7 and S9 conduct and output is $7V_{dc}+4V_{dc}+2V_{dc} =13V_{dc}=195V$ across the load.

Mode 15: Switches S2, S4, S6, S8 and S9 conduct and output voltage is $7V_{dc}+4V_{dc}+2V_{dc}+1V_{dc} =14V_{dc}=210V$ across the load.

As previously mentioned, it repeats in descending sequence from mode 14 to mode 1, providing the positive half cycle of the output voltage waveform with 29 levels. To create a negative half cycle, the same modes will recur. The output voltage waveform of the suggested MLI is displayed in Fig. 3, and the modes of operation for producing a positive half-cycle output waveform are displayed in Fig. 4. The modes of operation of the suggested MLI for producing an output waveform during the negative half cycle are displayed in Fig. 5. The suggested multilayer inverter's modes of operation are displayed in Table 1.

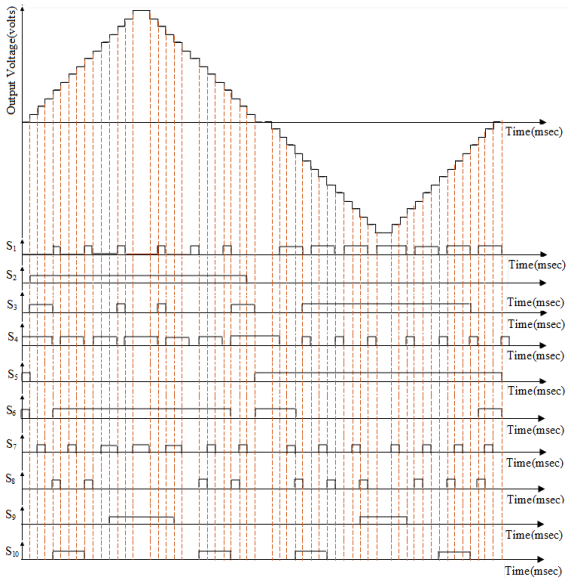


Fig. 3. Output voltage waveform of Proposed Multilevel Inverter

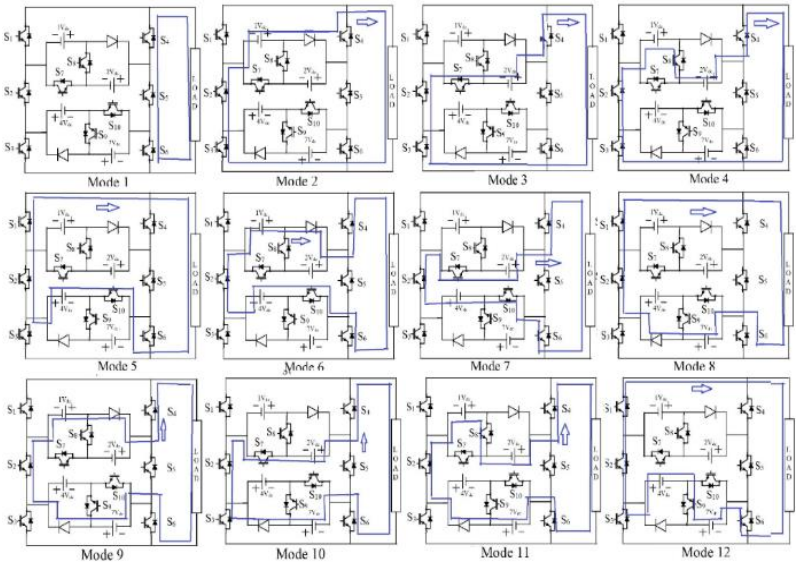


Fig. 4. Operation of Proposed MLI for producing positive half cycle

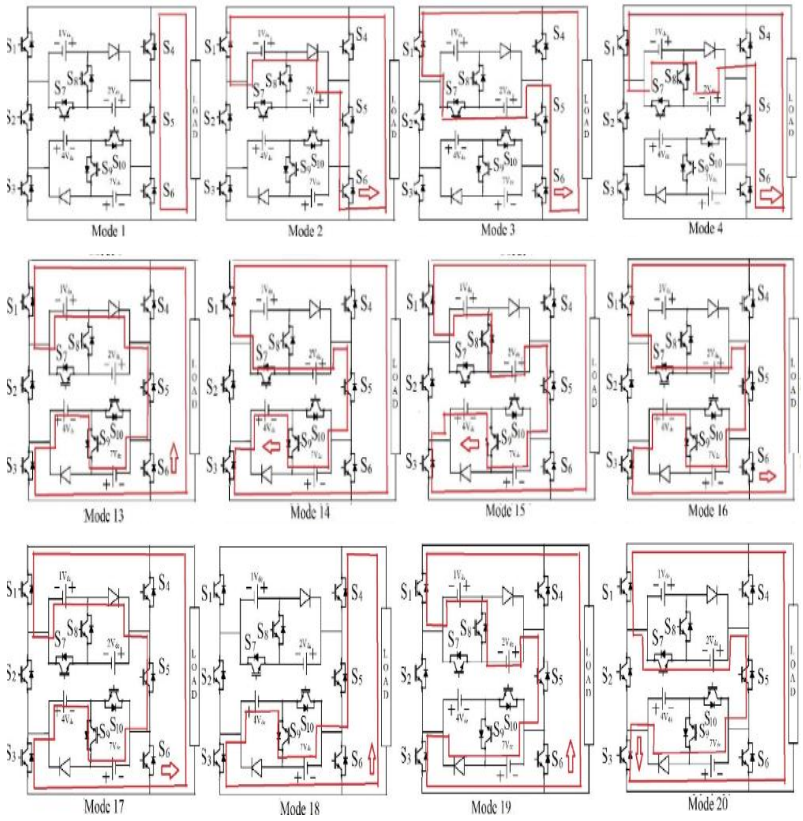


Fig. 5. Operation of Proposed MLI for producing negative half cycle

Table 1. Operation of Proposed Multilevel Inverter

	Modes	Load current path										Output Voltage(V)	
		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10		
Positive Half Cycle	1	0	0	0	1	1	1	0	0	0	0	0Vdc	0V
	2	0	1	1	1	0	0	0	0	0	0	1Vdc	+15V
	3	0	1	1	1	0	0	1	0	0	0	2Vdc	+30V
	4	0	1	1	1	0	0	0	1	0	0	3Vdc	+45V
	5	1	1	0	0	0	1	0	0	0	1	4Vdc	+60V
	6	0	1	0	1	0	1	0	0	0	1	5Vdc	+75V
	7	0	1	0	1	0	1	1	0	0	1	6Vdc	+90V
	8	0	1	0	1	0	1	0	1	0	1	7Vdc	+105V
	9	1	1	0	0	0	1	0	0	0	0	8Vdc	+120V
	10	0	1	0	1	0	1	0	0	0	0	9Vdc	+135V
	11	0	1	0	1	0	1	1	0	0	0	10Vdc	+150V
	12	0	1	0	1	0	1	1	0	1	0	11Vdc	+165V
	13	1	1	1	0	0	1	0	0	1	0	12Vdc	+180V
	14	0	1	0	1	0	1	0	0	1	0	13Vdc	+195V
	15	0	1	0	1	0	1	1	0	1	0	14Vdc	+210V
	16	0	1	0	1	0	1	0	0	1	0	13Vdc	+195V
	17	1	1	1	0	0	1	0	0	1	0	12Vdc	+180V
	18	0	1	0	1	0	1	1	0	1	0	11Vdc	+165V
	19	0	1	0	1	0	1	1	0	0	0	10Vdc	+150V
	20	0	1	0	1	0	1	0	0	0	0	9Vdc	+135V
	21	1	1	0	0	0	1	0	0	0	0	8Vdc	+120V
	22	0	1	0	1	0	1	0	1	0	1	7Vdc	+105V
	23	0	1	0	1	0	1	1	0	0	1	6Vdc	+90V
	24	0	1	0	1	0	1	0	0	0	1	5Vdc	+75V
	25	1	1	0	0	0	1	0	0	0	1	4Vdc	+60V

	26	0	1	1	1	0	0	0	1	0	0	3Vdc	+45V
	27	0	1	1	1	0	0	1	0	0	0	2Vdc	+30V
	28	0	1	1	1	0	0	0	0	0	0	1Vdc	+15V
	29	0	0	0	1	1	1	0	0	0	0	0Vdc	0V
Negative Half Cycle	1	0	0	0	1	1	1	0	0	0	0	0Vdc	0V
	2	1	0	0	0	1	1	0	0	0	0	-1Vdc	-15V
	3	1	0	0	0	1	1	1	0	0	0	-2Vdc	-30V
	4	1	0	0	0	1	0	0	1	0	0	-3Vdc	-45V
	5	0	0	1	1	1	0	0	0	0	1	-4Vdc	-60V
	6	1	0	1	0	1	0	0	0	0	1	-5Vdc	-75V
	7	1	0	1	0	1	0	1	0	0	1	-6Vdc	-90V
	8	1	0	1	0	1	0	0	1	0	1	-7Vdc	-105V
	9	0	0	1	1	1	0	0	0	0	0	-8Vdc	-120V
	10	1	0	1	0	1	0	0	0	0	0	-9Vdc	-135V
	11	1	0	1	0	1	0	1	0	0	0	-10Vdc	-150V
	12	1	0	1	0	1	0	0	1	0	0	-11Vdc	-165V
	13	0	0	1	1	1	0	0	0	1	0	-12Vdc	-180V
	14	1	0	1	0	1	0	0	0	1	0	-13Vdc	-195V
	15	1	0	1	0	1	0	1	0	1	0	-14Vdc	-210V
	16	1	0	1	0	1	0	0	0	1	0	-13Vdc	-195V
	17	0	0	1	1	1	0	0	0	1	0	-12Vdc	-180V
	18	1	0	1	0	1	0	0	1	0	0	-11Vdc	-165V
	19	1	0	1	0	1	0	1	0	0	0	-10Vdc	-150V
	20	1	0	1	0	1	0	0	0	0	0	-9Vdc	-135V
	21	0	0	1	1	1	0	0	0	0	0	-8Vdc	-120V
	22	1	0	1	0	1	0	0	1	0	1	-7Vdc	-105V
	23	1	0	1	0	1	0	1	0	0	1	-6Vdc	-90V
	24	1	0	1	0	1	0	0	0	0	1	-5Vdc	-75V
	25	0	0	1	1	1	0	0	0	0	1	-4Vdc	-60V
	26	1	0	0	0	1	0	0	1	0	0	-3Vdc	-45V
	27	1	0	0	0	1	1	1	0	0	0	-2Vdc	-30V
	28	1	0	0	0	1	1	0	0	0	0	-1Vdc	-15V
	29	0	0	0	1	1	1	0	0	0	0	0Vdc	0V

This section gives a brief synopsis of the main ideas and techniques that went into building and testing our system. Our approach's robustness and repeatability can be better understood by detailing the materials and procedures that were used. Fig.1 shows the block diagram of the proposed systems and Figure illustrates the schematic diagram of the suggested method.

2.1. PWM FOR HARMONIC REDUCTION

In multi-level inverters, the PWM technique is most frequently employed to remove detrimental low-order harmonics (Jing Zhao, 2010). In PWM control, the output voltage is adjusted by altering the pulse width, and switches are continually turned on and off for both positive and negative half cycles (Ismail, 2006). Inverter circuits frequently employ sinusoidal PWM as a control technique. Low switching losses, less output harmonics, and ease of implementation are some of its benefits. Its benefits include minimal switching losses, a less harmonic output waveform, and an easy-to-implement methodology. Constant amplitude pulses with a distinct duty cycle for each cycle are used to calculate the sinusoidal PWM. These pulses are produced

in order to reduce the output's harmonic content and achieve the necessary output voltage control. The most popular technique for inverter-fed electric drive-controlled applications is sinusoidal PWM (Ismail, 2006, Jing Zhao, 2010). A programmed SPWM is utilized to achieve the necessary switching angles, and the suggested multistage inverter performs at the desired output with amplitude and decreased harmonic content. It is demonstrated that the "n+1" equation is exacting in its control of the output voltage and the removal of "n" harmonics. The 29-level inverter's lower order harmonic removal technique is described. We found solutions for fourteen distinct angles.

The output voltage waveform's Fourier series may be extended using the following simple frequency conversion method: The friction coefficient is determined by Eq. 4 for compressible and completely turbulent flow (Abdul-Abbas et al., 2021, Tolbert, 1998).

$$V_o(\omega t) = \sum_{n=1,3,5}^{\infty} \frac{4V_{dc}}{n\pi}(\cos(n\theta_1)) + \cos(n\theta_2) + \cdots + \cos(n\theta_K))\sin(n\omega t) \quad (4)$$

where K is the number of switching angles needed for the inverter with 29 levels. It is necessary to determine the switching angles $\theta_1, \theta_2, \ldots, \theta_K$ for a specific fundamental voltage V1. So that a certain higher harmonic of Vn(nωt) equals zero and the output voltage Vo(ωt)=V1sin(ωt). The following formulas can be used to solve the switching angles.

$$\begin{gathered}\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) + \cos(\theta_4) + \cos(\theta_5) + \cos(\theta_6) = m \\ \cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) + \cos(5\theta_4) + \cos(5\theta_5) + \cos(5\theta_6) = 0 \\ \cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) + \cos(7\theta_4) + \cos(7\theta_5) + \cos(7\theta_6) = 0 \end{gathered} \quad (5)$$

Where modulation index, $m = \frac{V_1}{(\frac{4V_{dc}}{\pi})}$

The fifth, seventh, eleventh, thirteenth, seventeenth, nineteenth, twenty-third, and so on harmonic components will not be present in the output voltage of the 29-level inverter. Iterative techniques like the Newton-Raphson method (Corzine and Baker, 2002) are used to solve the set of non-linear transcendental Eq.5. The current methodology, in contrast to the iterative method, is based on employing resultant theory to solve polynomial equations, producing all potential solutions (Peng, 2004). It is possible to transform the transcendental equation that describes the harmonic content into a polynomial equation. Solutions are then found when they become available using the resultant approach. The total harmonic distortion (THD) of each of these solution sets must be examined in order to determine which one provides the least amount of harmonic distortion, mostly from the fifth, seventh, and eleventh harmonics.

THD is calculated as a percentage determined by

$$THD\% = \frac{\sqrt{V_3^2 + V_5^2 + V_7^2 + \cdots + V_{19}^2}}{V_1^2} \times 100 \quad (6)$$

3. RESULTS AND DISCUSSION

Through MAT Lab simulation for resistive load, the suggested multilevel inverter's performance is confirmed. For 29 levels, the total single-phase peak voltage is 210 V.

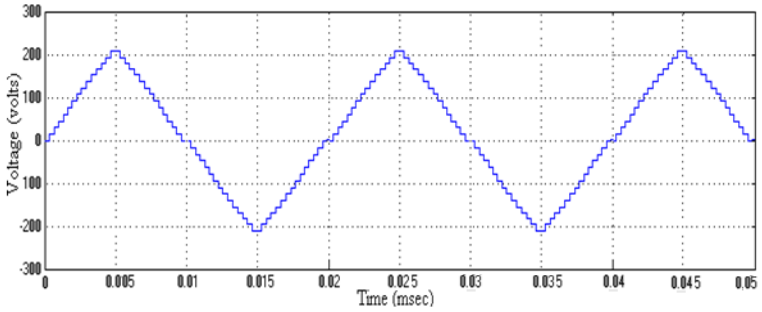


Fig. 6 Simulation Output voltage waveform for 29 level

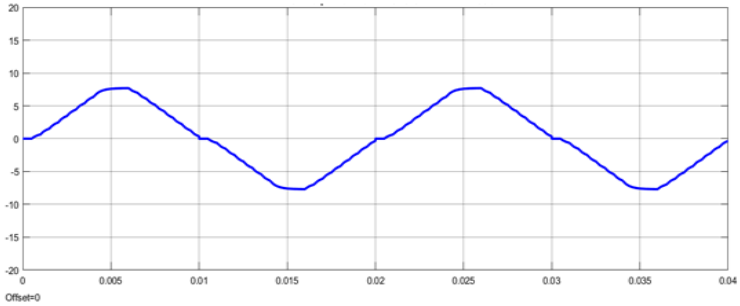


Fig. 7 Simulation Output current waveform for RL Load

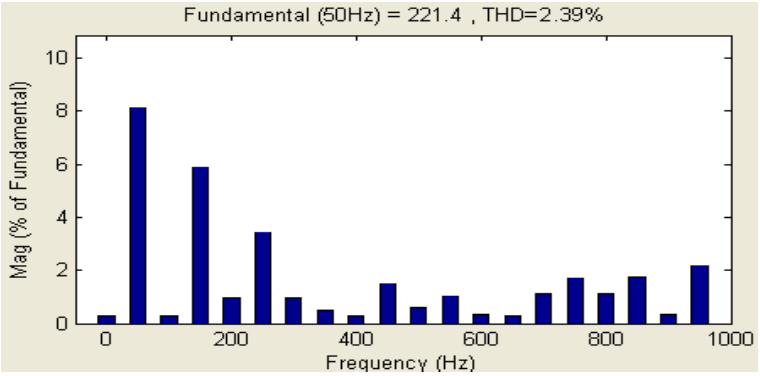


Fig. 8 Simulation -FFT Analysis

The output voltage waveform for 29 levels is displayed in Fig. 6. The output is a twenty-nine-level waveform that seems almost sinusoidal, as this image makes evident. Results of proposed MLI has been verified for Resistive Inductive (RL) load of real power – 2MW & reactive power -250VAR, Fig.7 shows the output current waveform for RL load. A 29-level inverter's THD value is 2.39%, as seen in Fig. 8. Hardware configuration validates simulation findings. A 210V, single phase, twenty-nine level recommended architectural prototype uses MOSFETs as switching devices. Ten MOSFET switches make up the inverter. In the hardware configuration, IRF840 MOSFETs are used. The Ardiuno micro controller generates the gate signal for inverter switches. The suggested 29-level inverter has four asymmetric DC sources installed on its input side: 15V, 30V, 60V, and 105V. A resistive load (3K-50W) is powered by the recommended

inverter output. The resistive load's hardware output voltage waveform is displayed in Fig. 9, and the output current waveform for the same load is displayed in Fig. 10. In Fig. 11, the experimental THD is displayed. According to this analysis, THD is 2.44 percent, which is less than the IEEE THD norm of 5%. The harmonics and overall harmonic distortion will decrease as the number of levels rises.

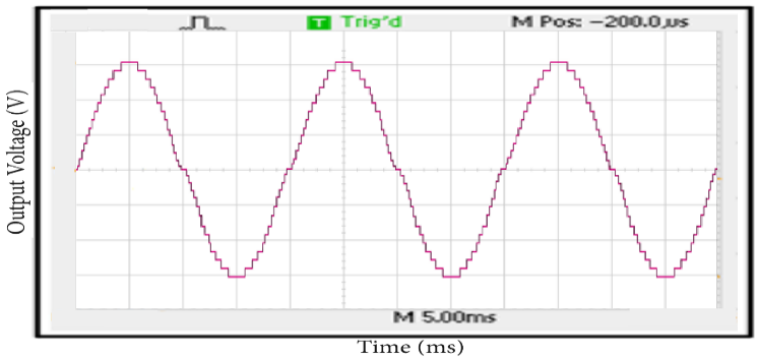


Fig. 9 Experimental output voltage for R load

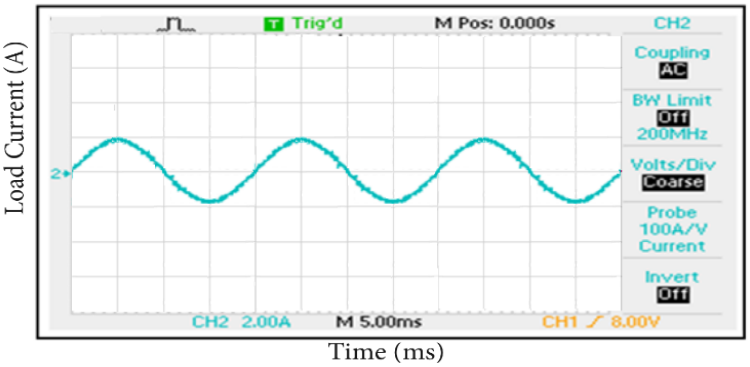


Fig. 10 Experimental output current for R load

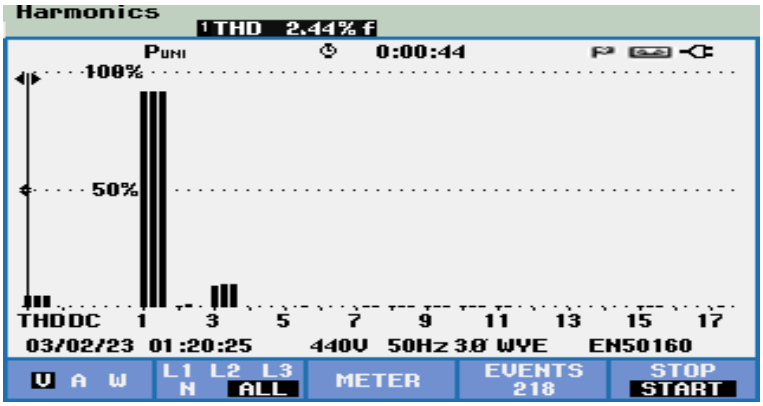


Fig. 11 Experimental THD

4. CALCULATION OF COST FUNCTION.

The total standing voltage of projected multilevel inverter is calculated as follows:

Total Standing Voltage = $\sum_{i=1}^{n} MBV_{Si}$

$TSV = MBV_{S1} + MBV_{S2} + MBV_{S3} + MBV_{S4} + MBV_{S5} + MBV_{S6} + MBV_{S7} + MBV_{S8}$

$TSV = 11V_{dc} + 5.5V_{dc} + 11V_{dc} + 11V_{dc} + 5.5V_{dc} + 11V_{dc} + 0V_{dc} + 0V_{dc} + 4V_{dc}$

$TSV = 59V_{dc}$

$TSV_{PU} = \frac{TSV}{MBV} = \frac{59V_{dc}}{14V_{dc}} = 4.214$

The Cost function of the proposed MLI calculated by equation (26),

$$\text{Cost Function} = (N_{SWT} + N_{Driv} + N_{Di} + N_{Cap} + \alpha TSV_{PU}) \times N_{DCS}$$

Cost function is,

$N_S = 10$, $N_{Driv} = 10$, $N_{Di} = 2$, $N_{Cap} = 0$, $\alpha = 0.5$ and $N_{DC} = 4$

$$\text{Cost Function} = (10 + 10 + 2 + 0 + 1 \times 4.214) \times 4 = 96.428$$

Cost function per level is calculated as,

$$\text{CF/Level} = \frac{\text{CF}}{\text{Number of Levels}} = \frac{96.428}{29} = 3.325$$

Cost function is,

$N_S = 10$, $N_{Driv} = 10$, $N_{Di} = 2$, $N_{Cap} = 0$, $\alpha = 1$ and $N_{DC} = 4$

$$\text{Cost Function} = (10 + 10 + 2 + 0 + 1 \times 4.214) \times 4 = 104.56$$

$$\text{CF/Level} = \frac{\text{CF}}{\text{Number of Levels}} = \frac{104.56}{29} = 3.616$$

5. COMPARISON OF MULTILEVEL INVERTERS

Comparison of various existing MLIs are done based on the switches, diodes, capacitors, driver circuits, DC sources and total standing voltage per unit. Table 2. shows that TSV per unit for the proposed 27 level MLIs is 4.214 when compare to the other existing MLIs. Number of switches used also 10 and diodes required is 2 and there four unsymmetrical DC sources. Cost function per level is also 3.32 only for cost coefficient 0.5 and cost function per level is 3.616 for cost coefficient 1. Fig.11 shows the comparison chart of various MLIs based on the switches and TSV per unit.

Table 2. Performance Comparison of Conventional and Proposed MLI

Topologies	Levels	N_{SWT}	N_{Di}	N_{cap}	N_{Driv}	N_{DCS}	MBV	TSV_{pu}
[18]	31	18	0	4	18	18	$15V_{dc}$	5.66
[19]	31	12	0	4	10	3	$15V_{dc}$	5.87
[20]	31	16	2	4	16	2	$15V_{dc}$	5.67
[21]	31	10	0	0	10	4	$15V_{dc}$	5.12
[22]	33	22	16	0	0	9	$16V_{dc}$	9.50
[23]	33	24	15	0	0	9	$16V_{dc}$	9.63
[24]	33	14	14	0	8	5	$16V_{dc}$	4.38
[25]	33	16	11	0	0	7	$16V_{dc}$	6.00
[26]	33	20	13	0	0	9	$16V_{dc}$	10.56
[27]	33	12	12	0	0	7	$16V_{dc}$	5.88
Proposed	29	10	2	0	10	4	$14V_{dc}$	4.214

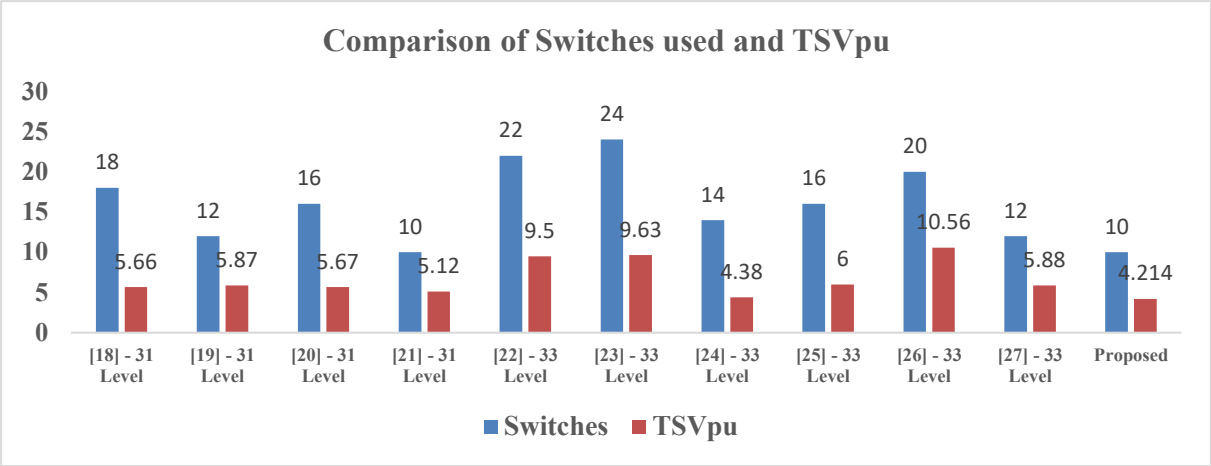


Fig. 12 Performance Comparison of MLIs

4. CONCLUSION

A novel multi-level inverter with reduced power components is the subject of this essay. The circuit and functioning of this multi-level inverter have been explained. In the traditional arrangement, the number of necessary power components rises in tandem with the number of output levels. More power switches are used, which raises THD, costs, switch losses, and harmonics. The suggested topology greatly decreases the power semiconductor switches to 10 for 29 nine levels. Total standing voltage of proposed MLIs is 4.214 and cost function per level is 3.325 for the weighted co-efficient of 0.5 and 3.616 for the weighted co-efficient of 1. Multi-level inverters are less complicated and less expensive overall because there are fewer devices. For electric vehicle applications, this suggested structure is therefore thought to be the most appropriate.

5. REFERENCES

Abdul-Abbas, Ali, and Shafaa Salih. "Comparison between LS-PWM and LPS-PWM for Switching-capacitor (SC) INVERTER". Kufa Journal of Engineering, vol. 9, no. 4, June 2021, pp. 146-162, https://doi.org/10.30572/2018/KJE/090410.

Ahmad A., M. Anas, A. Sarwar, M. Zaid, M. Tariq, J. Ahmad, and A. R. Beig (2020) "Realization of a generalized switched-capacitor multilevel inverter topology with less switch requirement", Energies, 13(7), 1556. doi.org/10.3390/en13071556

Alishah, R. S., Hosseini, S. H., Babaei, E. & Sabahi, M. (2016). Optimal design of new cascaded switch-ladder multilevel inverter structure, IEEE Transactions on Industrial Electronics, 64(3), 2072-2080, doi: 10.1109/tie.2016.2627019.

Amirreza, P.; Mehdi, N.; and Ali Emadi, (2021). “A Review of Multilevel Inverter Topologies in Electric Vehicles: Current Status and Future Trends”. IEEE Open Journal of Power Electronics, 2, 155-171. doi: 10.1109/ojpel.2021.3063550

Anssari, Othman. “A New Structure of Five-Level Diode Clamped Inverter with Reducing Its Elements”. Kufa Journal of Engineering, vol. 9, no. 4, June 2021, pp. 210-9, https://doi.org/10.30572/2018/KJE/090414.

Babaei, E., Laali, S. & Bayat, Z. (2015). A Single-Phase Cascaded Multilevel Inverter Based on a New Basic Unit with Reduced Number of Power Switches, IEEE Transactions on Industrial Electronics, 62(2), 922-929, doi: 10.1109/tie.2014.2336601.

Barzegarkhoo, R.; Forouzesh, M.; Lee, S. S.; Blaabjerg, F.; Siwakoti, Y. (2022). “Switched-Capacitor Multilevel Inverters: A Comprehensive Review”. IEEE Trans. on Power Electron. 37 (9), 11209 – 11243. doi: 10.1109/tpel.2022.3164508

Chiasson J.N.; Tolbert L.M.; Mckenzie K.J.; and Du Z. (2003). “Control of a Multilevel Converter Using Resultant Theory”. IEEE Transactions Control System Theory, 11(3), 345-354. doi: 10.1109/tcst.2003.810382

Corzine K. A.; and Baker J. R. (2002). “Reduced parts-count multilevel rectifiers”. IEEE Trans. Ind. Electron, 49(3), 766- 774. doi: 10.1109/tie.2002.801077

Corzine K. A.; Wielebski M. W.; Peng F. Z.; and Wang J. (2004). “Control of Cascaded Multilevel Inverters”. IEEE Trans. Power Electron, 19(3), 732-738. doi: 10.1109/tpel.2004.826495

Dhanamjayulu, C.; Arunkumar, G.; Jaganatha Pandian, B.; Padmanaban, S. (2020). “Design and implementation of a novel asymmetrical multilevel inverter optimal hardware components”. Inter. Trans. on Elec. Energy Sys. 30(2), e12201. doi.org/10.1002/2050-7038.12201

Ebrahimi, J., Babaei, E. & Gharehpetian, G. B. (2011). A new multilevel converter topology with a reduced number of power electronic components, IEEE Transactions on Industrial Electronics, 59(2), 655-667, doi: 10.1109/tie.2011.2151813.

Fracchia M.; Ghiara T.; Marchesoni M.; and Mazzucchelli M. (1992), “Optimized modulation techniques for the generalized N-level converter”. in proc. IEEE power electronics specialist conf, 1205-1213. doi: 10.1109/pesc.1992.254737

Hamidi, M. N.; Ishak, D.; Zainuri, M. A. A. M.; Ooi, C. A. (2020). "Multilevel inverter with improved basic unit structure for symmetric and asymmetric source configuration". IET Power Electron. 13(7), 1445-1455. doi.org/10.1049/iet-pel.2019.0916

Hosseinpour, M., Seifi, A. & Feyz, E. (2020). "A New Symmetric/Asymmetric Multilevel Inverter Based on Cascaded Connection of Sub-Multilevel Units Aiming less Switching Components and Total Blocked Voltage", Journal of Telecommunication, Electronic and Computer Engineering, 12(1), 53-62.

Hussan M. R., A. Sarwar, M. D. Siddique, S. Mekhilef, S. Ahmad, M. Sharaf, M. Zaindin, and M. Firdausi (2020). "A novel switched-capacitor multilevel inverter topology for energy storage and smart grid applications", Electronics, 9, (10), 1–18. doi.org/10.3390/electronics9101703

Ismail, S. T. (2006), "Development of a Single Phase SPWM Microcontroller- Based Inverter". First International Power and Energy Conference PEC, Putrajaya, Malaysia: IEEE, Nov, 28-29, doi: 10.1109/pecon.2006.346691

Jing Zhao. (2010), "A Novel PWM control method for hybrid-clamped multilevel inverters". IEEE Trans. Ind. Elec., 57(7), 2365 – 2373. doi: 10.1109/tie.2009.2027915

Kangarlu, M. F., Babaei, E. & Laali, S. (2012). Symmetric multilevel inverter with reduced components based on non-insulated dc voltage sources, IET Power Electronics, 5(5), 571–581, doi: 10.1049/iet-pel.2011.0263.

Manjrekar M. D.; Steimer P. K.; and Lipo T. A. (2000). "Hybrid multilevel power conversion system: a competitive solution for high- power applications". IEEE Trans. Ind. Applica, 36, 834-841. doi: 10.1109/ias.1999.805943

Meraj, S. T.; Hasan, K.; Masaoud, A. (2019). "A novel configuration of cross-switched T-type (CT-type) multilevel inverter". IEEE Trans. on Power Electron. 35(4), 3688-3696. doi: 10.1109/tpel.2019.2935612

Patel H.S.; and Hoft R.G.; (1973). "Generalized Techniques of Harmonic Elimination and Voltage Control in Thyristor Inverters: Part I – Harmonic Elimination". IEEE Trans. Ind. Appl., 3, 310-317. doi: 10.1109/tia.1973.349908

Peng F. Z. (2004), "A generalized multilevel inverter topology with self-voltage balancing". IEEE Trans. Ind. Applica, 37, 611- 618. doi: 10.1109/28.913728

Ravanan. S. D.; Arivukannu, S.; Tankappan, P.; and Muthiah, R. (2022). "Harmonic performance analysis of a wind driven micro grid inverter". International Journal of Ambient Energy, 43(1), 3497–3506. doi.org/10.1080/01430750.2020.1839547

Rodriguez, J.; Bernet, S.; P,Steimer, K.; and Lizama, I. E. (2010). "A survey on neutral-point-clamped inverters". IEEE Transactions on Industrial Electronics, 57(7), 2219–2230. doi: 10.1109/tie.2009.2032430

Rodriguez, J.; Lai, J. S.; and Peng, F. Z. (2002). "Multilevel inverters: a survey of topologies, controls and applications". IEEE Trans. Ind. Electron., 49(4), 724-738. doi: 10.1109/tie.2002.801052

Roy T., P. K. Sadhu, and A. Dasgupta (2019). "Cross-switched multilevel inverter using novel switched capacitor converters", IEEE Trans. Ind. Electron., 66, (11), 8521–8532. doi: 10.1109/tie.2018.2889632

Sahoo B., S. K. Routray, and P. K. Rout (2019). "Repetitive control and cascaded multilevel inverter with integrated hybrid active filter capability for wind energy conversion system", Eng. Sci. Technol., Int. J., 22, (3), 811–826. doi.org/10.1016/j.jestch.2019.01.001

Samadaei, E., Sheikholeslami, A., Gholamian, S. A. & Adabi, J. (2017). A square T-type (ST-type) module for asymmetrical multilevel inverters, IEEE Trans Power Electronics, 33(2), 987-996, doi: 10.1109/tpel.2017.2675381.

Tolbert, L. M.; and Peng, F. Z. (1999). "Multilevel converters for large electric drives". IEEE Trans. Ind. Appl., 35(1), 36-34. doi: 10.1109/28.740843

Tolbert, L. M.; Peng, F. Z.; and Habetler, T. G. (1998). "Multilevel inverters for electric vehicle applications". in Proc. Power Elect. Trans., 79–84. doi: 10.1109/pet.1998.731062