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RESEARCH ARTICLE

$SiO_2/Al_2O_3/HfO_2$ Selective Buried Oxide Layer (SELBOX) Engineering and Its Influence on 20 nm n-MOSFET

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Abstract

Miniaturizing Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) to the nanoscale results in specific structure and performance effects known as Short Channel Effects (SCEs). Performance degradation due to SCEs occurs due to increased leakage currents (IOFF), decreased threshold voltage (V_{TH}) stability and breakdown voltage. Various solutions for these problems have been developed through the application of structural and material engineering techniques. One particular engineering technique that shows promise as a potential solution is to incorporate a Selective Buried Oxide Layer (SELBOX). In this article, we investigate how the introduction of a SELBOX impacts the electrical characteristics of nano-scale n-MOSFETs through device simulation (TCAD). For the purposes of this study, we developed a 20 nm n-MOSFET with a high-k HfO_2 gate dielectric using the TCAD Silvaco ATLAS software package. Three different types of SiO_2, Al_2O_3, and HfO_2 dielectric materials were used in conjunction with the SELBOX layer which is located at a depth of 30 nm from the drain. In addition, the location of the SELBOX as related to the drain was also varied from its original position to the direct vicinity of the channel to assess the overall effect of the SELBOX position. Finally, we compare the characteristics of a conventional-type MOSFET (no SELBOX) to those of devices modified by inclusion of the SELBOX at varying positions/depths from the drain. The findings indicate that the dielectric constant and band gap of the implanted material, as well as its closeness to the drain and channel region, substantially influence device performance. In the instance of SiO_2 as SELBOX material, the I_{OFF} decreased by 33%, and the breakdown voltage significantly increased from 85.09 V to 491.4 V. The utilization of Al_2O_3 resulted in a 27% reduction in I_{OFF} and an increase in breakdown voltage from 85.09 V to 275.7 V. Notably, the application of HfO_2 as SELBOX material resulted in a divergent effect: I_{OFF} rose by 21%, but the breakdown voltage increased to 172.3 V.

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Keywords: Al_2O_3, HfO_2, n-MOSFET; SELBOX; Silvaco ATLAS; Breakdown Voltage.

1. Introduction

Integrated circuits rely heavily on the MOSFET as a result of its scalable nature, an economical price point and compatibility with CMOS processing technology [1]. The MOSFET is also utilised within the context of intelligent control systems [2], and during the process of creating efficient hybrid energy systems [3]. However, as channel lengths decrease towards nanoscale dimensions, short channel effects (SCEs), such as threshold voltage (V_{TH}) roll-off, drain-induced barrier lowering (DIBL) and increased leakage currents (I_{OFF}) begin to severely limit device performance and reliability. Therefore, these limitations require the creation of new solutions that provide electrostatic integrity, high drive current (ID) and minimal power consumption. Silicon-on-insulator (SOI) architectures and high-k gate dielectric materials have been proposed as some of the potential solution approaches. SOI MOSFETs utilize a buried oxide layer to diminish parasitic capacitance and leakage [4,5], although high-k materials like Al_2O_3 (k = 9, Eg = 8.8 eV) and HfO_2 (k = 25, Eg = 5.8 eV) are replacing traditional SiO_2 to facilitate additional scaling [6]. Although these methods have demonstrated efficacy, they mainly depend on global structural changes. Localized dielectric engineering has received insufficient attention, despite its potential to more effectively mitigate SCEs without the disadvantages associated with continuous buried oxides. Narayanan et al. [7] examined the kink effect in partially depleted SOI 2 µm MOSFETs and showed that the implantation of a 0.4 µm SELBOX structure beneath the source and drain efficiently mitigates the floating-body-induced kink. The work demonstrated using Silvaco ATLAS simulations that optimizing the length and thickness of the oxide gap diminishes the kink effect while maintaining the advantages of SOI, with a created device model offering more insights into the optimization of SELBOX parameters. Thakral et al. [8] examined the scaling difficulties of 28 nm SOI MOSFETs and discovered planar fully depleted SOI (FD-SOI) as an appropriate low-power substitute for bulk CMOS. Their TCAD-based research shown that the kink effect in partially depleted SOI (PD-SOI) devices may be effectively mitigated with the implementation of a 0.4 µm SELBOX structure, hence improving device reliability while maintaining the fundamental advantages of SOI technology. Narayanan et al. [9] introduced an enhanced 0.12 µm SOI MOSFET architecture using a 100 nm SELBOX beneath the source and drain to reduce self-heating issue. TCAD simulations validated that adjusting gap parameters significantly mitigates thermal effects while maintaining SOI performance advantages. Mahmoud et al. [10] constructed a 90 nm CMOS employing a 10 nm SELBOX via TCAD ATLAS and assessed the dynamic power relative to SOI CMOS and BULK CMOS. The total dissipated dynamic power across all individuals is equivalent at elevated frequencies. The dynamic power dissipation of the SOI and SELBOX structures was similar at low frequencies, both demonstrating lower

values than the BULK configuration. SELBOX CMOS eliminated the kink effect and self-heating, making it superior than SOI CMOS. The SELBOX MOSFET improves device efficiency by reducing power loss. Yoo and Kim [11] introduced a 45 nm buried oxide with a Buried Oxide Nano-sheet Field Effect Transistor (BO-NSFET) that situates the oxide exclusively beneath the gate region to mitigate substrate band-to-band tunneling (BTBT). According to TCAD studies, the proposed design provides a substantial reduction in IOFF and parasitic leakage versus traditional NSFETs allowing for improved performance at advanced nodes. Additionally, Murshid and Bashir [12] proposed a GP-SELBOX Junction Less Transistor to address the limitations of conventional SOI-JLTs operating at less than 20 nm nodes. The addition of a p-type ground plane and a 10 nm SELBOX to the device structure provides greater depletion, reduced leakage, improved ION/IOFF ratio, better SCE management while maintaining comparable cutoff frequency and less self-heating.

This research demonstrates how newly designed layers of SELBOX layer engineering for nanoscale MOSFETs can optimize performance through material choice and vertical positioning of the dielectric material layer. The study also demonstrates that using a high band gap dielectrics material such as SiO_2 in the near channel-drain junction location, will reduce leakage current by as much as 33%, and increase the breakdown voltage over five times compared to the conventional designs. Results indicate that Al_2O_3 provides a moderate improvement in performance, while HfO_2 demonstrates the limitations of using lower bandgap dielectrics material in the same position. These results point to an important new avenue of investigation: the interaction between buried dielectric materials properties and their spatial position has the potential to create new options for optimization of device performance in advanced technology nodes with short channels.

2. Methodology

This study employs TCAD Silvaco ATLAS to model and study an n-channel MOSFET at the nanoscale. The W/L ratio of this structure is 100 nm/20 nm. Use of a high-k gate dielectric such as HfO_2 also helps to achieve low gate leakage characteristics of this device while maintaining excellent electrostatic control of the channel, as shown in Table 1 which lists the primary parameters investigated by [8].

TABLE 1. Parameters of design 20 nm n-MOSFET.

Parameters	Value
Channel	20 nm Si
Doping of Source and Drain	$5 \times 10^{20}\ cm^{-3}$
Doping of Channel	$9 \times 10^{17}\ cm^{-3}$
Doping of Substrate	$1 \times 10^{14}\ cm^{-3}$
Gate Workfunction	4.55ev
Gate length	25 nm
Source and Drain Length	40 nm
Gate Dielectric Thickness	10 nm

Correct model selection is critical in the structure of this simulation. In this work, the Auger (three carriers) and SRH (fixed minority carrier lifetime) models are used for the direct transitions. The Arora Model replaces the ANALYTIC model for Si, and the CVT method applies to the overall system. The numerical solver, Newton-Gummel with trap autonr, gives consistently better starting estimates compared to more complex situations.

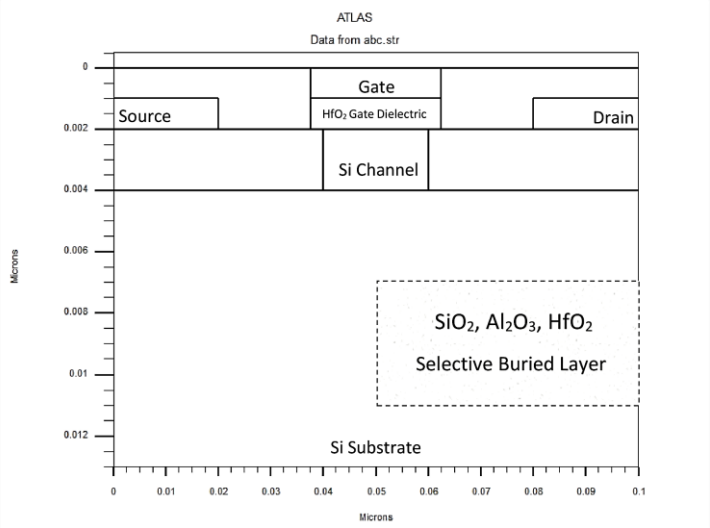

Fig. 1. Schematic View of insertion selective buried oxide layer (SELBOX) in 20 nm n-MOSFET.

The selective oxide layer (SELBOX) for our research is a crucial component and is located within the silicon substrate. At a thickness of 40nm and located at 30nm, the SELBOX extends from 50nm to 100nm in the lateral dimension along the x-axis. Three distinct dielectric materials are utilized independently for the SELBOX in different models: SiO_2, Al_2O_3, and HfO_2 as shown in Figure 1. This facilitates a comparative assessment of the impact of each dielectric material and band gap value on the device concerning SCEs. In succeeding modeling, the SELBOX is elevated in the upward direction until it achieves direct contact with the active channel region. The use of various materials and vertical repositioning is conducted to assess how the closeness of the SELBOX to the channel affects electric field distributions and whole device performance.

3. Results and Discussion

3.1. SiO_2 material (k=3.9 and band gap=9 eV)

This study assesses the electrical properties of 20 nm n-MOSFET devices with SiO_2 SELBOX depths of 30 nm, 20 nm, 10 nm, and direct contact position with the channel, in comparison to a standard design of 20 nm n-MOSFET (without a SELBOX). The primary parameters evaluated comprise threshold voltage (V_{TH}), ON current (I_{ON}), OFF current (I_{OFF}), I_{ON}/I_{OFF} ratio, breakdown voltage, and Drain-Induced Barrier Lowering (DIBL).

Table 2 illustrates that the V_{TH} exhibits remarkable stability across all SELBOX positions, with minimal variations from 0.462 V in the standard design to 0.461 V in the direct contact position, that means the substrate coupling not affected, in order to the electrostatics in the channel stay steady. The slight fluctuation indicates that the vertical placement of the SiO_2 SELBOX minimally affects the V_{TH}, which is beneficial for preserving device switching stability.

TABLE 2. Main parameters of (standard design of n-MOSFET) and the influence of SiO_2 selective buried oxide layer (SELBOX) at (30 nm depth, 20 nm depth, 10 nm depth and direct contact position).

Parameters	Standard	30 nm Depth	20 nm Depth	10 nm Depth	Direct Contact
V_{TH} (V)	0.462	0.454	0.456	0.458	0.461
$I_{ON} \times 10^{-3}$ (A/m)	2	2.12	2.11	2.10	2.07
$I_{OFF} \times 10^{-11}$(A/m)	8.5	10	8.89	7.24	5.68
$I_{ON}/I_{OFF} \times 10^{7}$	2 .37	1.98	2.37	2.90	3.65
Breakdown Voltage (V)	85.09	137.1	199.3	312.5	491.4
DIBL (mV/V)	308	307	306	304	302

The I_{ON} exhibits a little fluctuation with alterations in SELBOX depth. Raising the SELBOX depth from 30 nm to 10 nm improves electrostatic gate control over the channel, elevating I_{ON} from 2.00×10^{-3} A/m in the standard design to 2.12×10^{-3} A/m at 30 nm depth. When the SELBOX is in direct contact with the channel, I_{ON} diminishes to 2.07×10^{-3} A/m, indicating a decline in effective gate control caused by the modified field distribution inside the device's bulk [14].

Conversely, the I_{OFF} has a greater degree of fluctuation. The implanting of a SELBOX at a depth of 30 nm elevates I_{OFF} from 8.5×10^{-11} A/m at standard design to 1.0×10^{-10} A/m at 30 nm depth. The improved performance of the fringing fields around the source/drain regions and additional junction leakage due to their physical distance from the substrate explains the increase in performance. In particular, the decrease in the drain-source-off current (I_{OFF}) to 5.68×10^{-11} A/m due to improved isolation and reduction in leakage paths from the substrate (the SELBOX is placed in direct contact) is another example of the benefits of using this configuration [15].

The I_{ON}/I_{OFF} ratio significantly enhances, attaining 3.65×10^{7} in the direct contact position, in contrast to 2.37×10^{7} in the standard MOSFET. This illustrates exceptional switching performance and indicates that the revised SELBOX positioning improves the equilibrium between I_{ON} performance and I_{OFF} mitigation. A significant enhancement is noted in the breakdown voltage, rising from 85.09 V in the standard design to 491.4 V upon direct contact of the SELBOX with the channel. This improvement results from the diminished fringing fields at the drain side, coupled with the high bandgap (about 9 eV) of SiO_2 and its insulating barrier effect, which decreases the vertical electric field within the substrate and enhances dielectric robustness. As a result, leakage is further reduced, and the MOSFET attains markedly improved dependability [16] [17].

Throughout all configurations, the DIBL values are approximately 306 mV/V indicating that the placement of the SiO_2 SELBOX is more important in terms of leakage and breakdown character than it is for electrostatic stability.

As illustrated in Figure 2, there is a distribution of electric fields from the placement of the SiO_2 SALBOX, which causes an increase in the fringing electric field at the source side at 30 nm down from the surface of the device compared to the large amount of fringing electric field present at the drain side. This is because the oxide layer prohibits the passage of electric fields through it, this results in perturbing the potential distribution throughout the monolithic device, as it will bend upwards towards the area of electric field concentration.

Moreover, the density of the field lines above the buried oxide layer is substantially less than the field lines below the oxide layer. This phenomenon can be attributed to the shielding—or partially shielding—effect of the buried oxide.

As the SELBOX is raised from a depth of 30 nm to a direct contact position beneath the drain region, the field distribution exhibits significant enhancements. The source side fringing fields have diminished, and the SELBOX now functions as a more robust barrier against electric field entry into the substrate, efficiently directing and reducing substrate coupling. At the drain side, the electric field intensity at the drain-substrate interface becomes higher, while the oxide isolation considerably diminishes field entry into the bulk silicon, therebyavoiding early breakdown of the device. The enhanced field confinement results in a significant rise in breakdown voltage, as verified by Table 2, which shows breakdown voltage rising from 85.09 V in the standard design to 491.4 V with direct contact to the SELBOX.

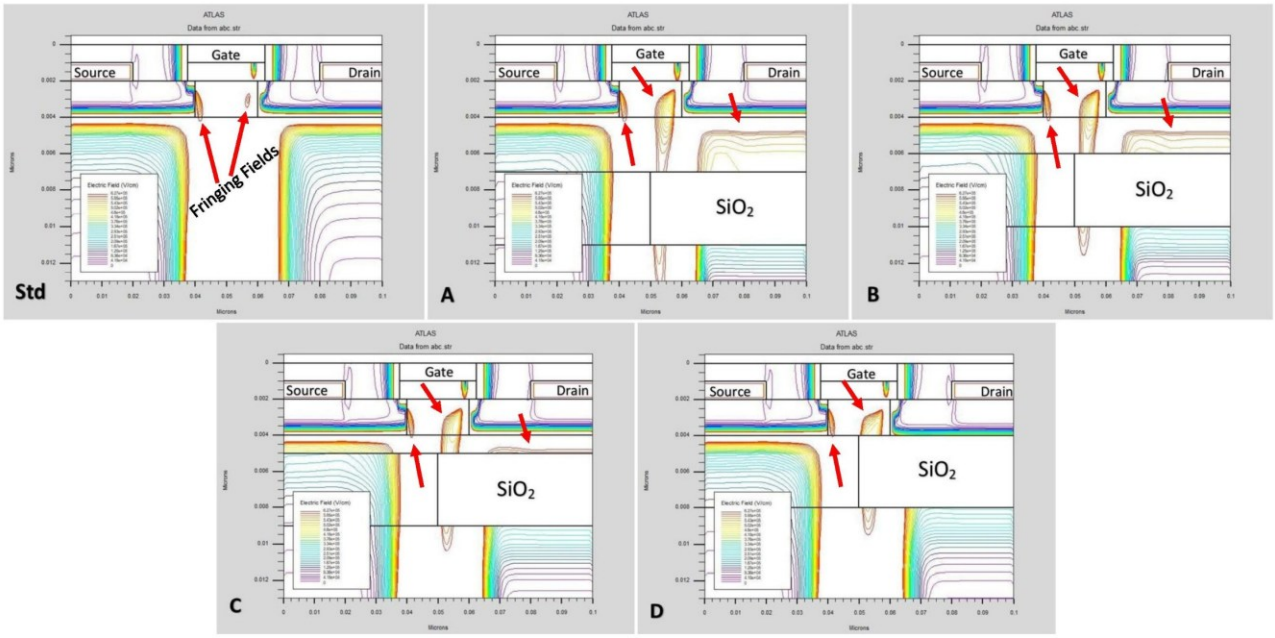

Fig. 2. Electric field distribution at (standard design of n-MOSFET) and SiO_2 selective buried oxide layer (SELBOX) at (30 nm depth, 20 nm depth, 10 nm depth and direct contact position).

3.2. Al_2O_3 material (k=9 and band gap=8.8 eV)

This investigation assesses the performance of MOSFET devices utilizing Al_2O_3 as the SELBOX at depths of 30 nm, 20 nm, 10 nm, and in direct contact with the channel, in comparison to a conventional design.

The data presented in Table 3 displays strong stability of the V_{TH} value in each of the different types of SELBOX designs, with the V_{TH} fluctuating, but only by 0.003 V, between 0.461 and 0.464 across the various designs. Therefore, it can be concluded that the use of Al_2O_3 for the SELBOX does not negatively impact the electrostatics of the channel or the amount of control exerted by the gate over the channel. In addition, the high dielectric constant value (K = 9) for Al_2O_3 provides superior gate-to-channel modulation and also minimizes the effects of SCE. Therefore, the stability of the VTH demonstrates that Al_2O_3 can provide the necessary reliable switching performance in modern CMOS designs.

In terms of I_{ON} performance, the values for ION are stable and robust throughout the range of designs with only minor fluctuations as compared to the standard design. At all depths of SELBOX, including the depth of direct contact between the SELBOX and the substrate, the value of I_{ON} for the Al_2O_3 SELBOX was recorded at 2×10^{-3} A/m. The data indicates that the high dielectric constant of Al_2O_3 provides adequate electrostatic gate control; therefore, when the oxide layer is positioned closer to the drain, the electrostatic force produced will keep the inverter inversion due to charge response for the Al_2O_3 oxide intact. In contrast to the Al_2O_3 findings, the SiO_2 SELBOX had a slight decrease in the value of ION when the oxide was in direct contact with the substrate, indicating that the Al_2O_3 has a greater ability to maintain a strong inversion charge density and ION capability.

As the SELBOX is elevated from 30 nm deep (8.52×10^{-11} A/m, the I_{OFF} drops to 6.20×10^{-11} A) to the point of direct contact, the I_{OFF} decreases. This increase in performance occurs because of decreasing fringing electric fields in the space adjacent to the drain junction, and the increased physical separation of leakage paths between the source/drain and substrate. The I_{ON}/I_{OFF} ratio markedly increases from 2.37×10^7 in the standard design to 3.24×10^7 upon direct contact position, indicating enhanced switching efficiency with minimal reduction in I_{ON}.

Compared to a standard SELBOX design of 85.09 V based on traditional dielectric materials and structures, the breakdown voltage increases significantly from 85.09 V to 275.7 V with a device constructed using improved technology to create a direct contact position. The increased breakdown voltage is attributed to the high-k material used, which is the Al_2O_3 insulation layer, allowing for a lower leakage of vertical electric fields into the substrate and improving the insulation between junctions. While Al_2O_3 has an energy band gap of approximately 8.8 eV, which is slightly lower than that of SiO_2 (approximately 9 eV), it can still effectively reduce high-field stress and prevent leakage from junctions. However, while the increase in breakdown voltage compared to devices created using SiO_2 based configurations is only slight, this indicates the importance of the trade-off between dielectric material band gap and dielectric permittivity when designing dielectric structures. Although Al_2O_3 provides a small reduction in leakage compared to SiO_2, it provides a substantial increase in breakdown voltage; however, it does not provide the same level of increase as SiO_2 based SELBOX designs. DIBL remains approximately consistent at 308 mV/V across all configurations, indicating that variations in SELBOX position and oxide material selection predominantly influence leakage and breakdown performance rather than the integrity of electrostatic gate channel control.

TABLE 3. Main parameters of (standard design of n-MOSFET) and the influence of Al_2O_3 selective buried oxide layer (SELBOX) at (30 nm depth, 20 nm depth, 10 nm depth and direct contact position).

Parameters	Standard	30 nm Depth	20 nm Depth	10 nm Depth	Direct Contact
V_{TH} (V)	0.462	0.461	0.462	0.463	0.464
$I_{ON} \times 10^{-3}$ (A/m)	2	2.03	2.03	2.02	2.01
$I_{OFF} \times 10^{-11}$(A/m)	8.5	8.52	7.97	7.25	6.20
$I_{ON}/I_{OFF} \times 10^7$	2 .37	2.38	2.53	2.79	3.24
Breakdown Voltage (V)	85.09	130.5	155.7	198.7	275.7
DIBL (mV/V)	308	308	307	307	306

Figure 3 depicts the alterations in the electric field profile resulting from the relocation of the Al_2O_3 SELBOX. At a depth of 30 nm, the SELBOX induces a minor enhancement of fringing fields on the drain side, attributable to localized field crowding near the drain junction. As the SELBOX is elevated nearer to the drain, surrounding fields diminish consistently, exhibiting substantial suppression at the position of direct contact. The electric field scattering over the Al_2O_3 SELBOX is practically eliminated, illustrating the oxide's excellent insulating capability.

By reallocating electric field lines, the overall durability of electric field devices increases since vertical electric field penetration into the substrate is reduced. As a result, the amount of leakage path through the substrate is decreased and additional electric breakdown voltage is created. Dual gate (also known as Al_2O_3 relaxed dielectric) SELBOX can maintain minimal values of IOFF without compromising electric field confining effect. Therefore, this facilitates the use of electric field devices in scaled MOSFET architectures where oxide engineering plays a critical role in the maximization of ION, IOFF, and device reliability.

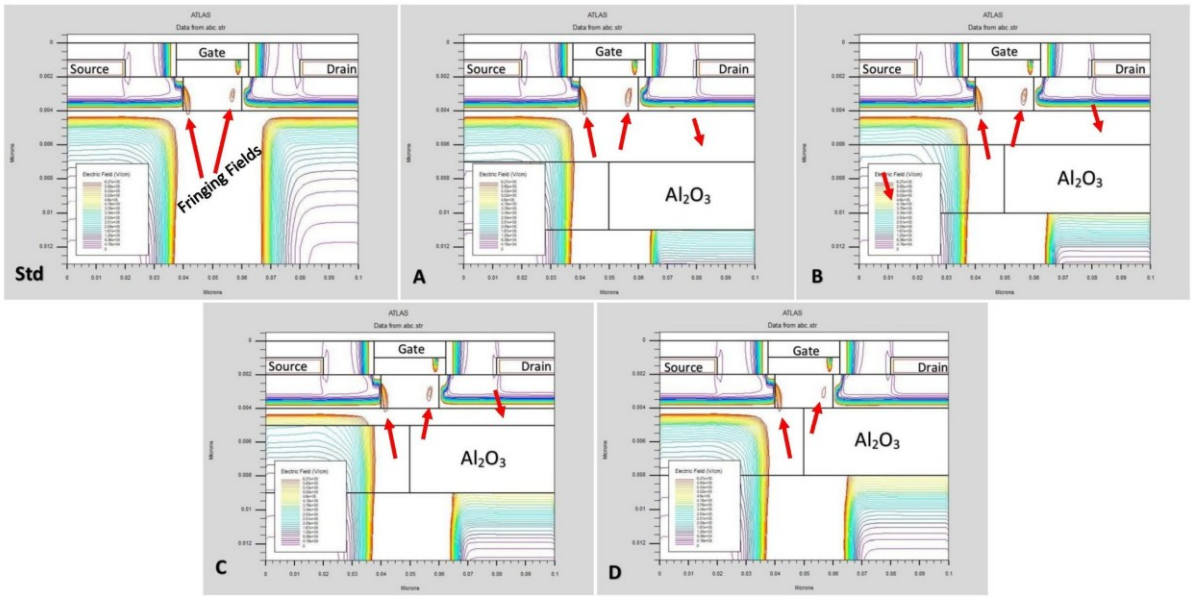

Fig. 3. Electric field distribution at (standard design of n-MOSFET) and Al_2O_3 selective buried oxide layer (SELBOX) at (30 nm depth, 20 nm depth, 10 nm depth and direct contact position).

3.3. HfO_2 material (k=25 and band gap=5.8 eV)

This section examines the influence of different HfO_2 SELBOX depths 30 nm, 20 nm, and 10 nm, along with a direct contact configuration, on the performance of MOSFET devices, compared to a standard design of MOSFET device.

Table 4 depicts that the V_{TH} exhibits a slight elevation with the implementation of the HfO_2 SELBOX, increasing from 0.462 V in the standard design to a peak of 0.470 V when the SELBOX is situated 30 nm beneath the drain region. The increase results from improved electrostatic confinement and less substrate coupling facilitated by the high-k HfO_2 layer, which reduces gate control over the channel at intermediate depths. As the SELBOX is elevated nearer to direct contact with the drain, V_{TH} marginally lowers to 0.464 V. This reduction signifies that, although HfO_2 improves vertical isolation, its closeness to the channel somewhat modifies the electric field distribution and diminishes gate-to-channel electrostatics, resulting in a modest decrease in V_{TH} [18].

The I_{ON} values are marginally diminished in comparison to the standard MOSFET structure with 2.00×10^{-3} A/m. The values fluctuate between 1.93×10^{-3} A/m and 1.97×10^{-3} A/m across all structures. The decrease is ascribed to the elevated dielectric constant and physical thickness of the SELBOX, which marginally diminishes inversion charge density and channel mobility by altering vertical electric fields. The little decrease in I_{ON} suggests that the integration of HfO_2 SELBOX entails a compromise in I_{ON} performance.

The I_{OFF} demonstrates a nonlinear pattern. Initially, it diminishes to 7.44×10^{-11} A/m at a SELBOX depth of 30 nm, due to diminished substrate coupling and efficient obstruction of leakage pathways. As the SELBOX approaches direct contact, I_{OFF} increases to 10.3×10^{-11} A/m, attributed to improved field penetration through the reduced substrate regions and leakage pathways along the SELBOX peripheries.

The I_{ON}/I_{OFF} ratio exhibits a trend, reaching a maximum of 2.61×10^7 at a depth of 30 nm, exceeding the standard design of 2.37×10^7, before decreasing to 1.91×10^7 upon direct contact position. The results indicate that a 30 nm SELBOX depth optimally suppresses leakage while sustaining acceptable I_{ON} levels, whereas direct contact, while enhancing breakdown voltage, and increases I_{OFF}.

HfO_2 SELBOX creates a drastic increase in the breakdown voltage through contact with HfO_2, going from the typical 85.09 V in design mode to 172.3 V in the direct contact mode. This increase is due to the larger dielectric constant of HfO_2 and the physical barrier to vertical electric field strength in the bulk substrate that results in the stability of HfO_2 devices. When compared with SiO_2 SELBOX devices, it should also be noted that HfO_2 has a lower bandgap (around 5.8 eV versus 9 eV), which limits the increase in maximum breakdown voltage, and thus, results in an increased IOFF, particularly when the oxide is positioned near the Drain region.

DIBL exhibits relative stability across all SELBOX depths at around 312 mV/V, indicating that although the selection and positioning of SELBOX materials significantly affect leakage and breakdown properties, electrostatic channel management remains uniform.
7.44×10^{-11} A/m at a SELBOX depth of 30 nm, subsequently rising to 10.3×10^{-11} A/m as the SELBOX's direct contact position is altered. This increase is attributed to the SELBOX facilitating leakage pathways between the source and drain regions and the substrate. The I_{ON}/I_{OFF} ratio attains its maximum at a depth of 30 nm, measuring 2.61×10^7, above the conventional design value of 2.37×10^7. However, it progressively decreases as the SELBOX is moved to the direct contact position, ultimately reaching 1.91×10^7. In comparison to the conventional MOSFET design, the breakdown voltage increases from 85.09 V to 172.3 V when a SELBOX is implanted at the direct contact location. The SELBOX first increases the breakdown voltage by creating an insulating barrier that reduces the vertical electric field in the bulk substrate. When the value of the band gap value became half of the band gap in first case, about 5.8 eV, and becoming closer

to the drain region, leading to a slight increment in the breakdown voltage, and an increase in the leakage current. DIBL values almost constant for all cases is approximately about 312 mV/V.

TABLE 4. Main parameters of (standard design of n-MOSFET) and the influence of HfO_2 selective buried oxide layer (SELBOX) at (30 nm depth, 20 nm depth, 10 nm depth and direct contact position).

Parameters	Standard	30 nm Depth	20 nm Depth	10 nm Depth	Direct Contact
V_{TH} (V)	0.462	0.470	0.468	0.466	0.464
$I_{ON} \times 10^{-3}$ (A/m)	2	1.94	1.95	1.93	1.97
$I_{OFF} \times 10^{-11}$(A/m)	8.5	7.44	8.76	10	10.3
$I_{ON}/I_{OFF} \times 10^{7}$	2 .37	2.61	2.22	1.95	1.91
Breakdown Voltage (V)	85.09	111.6	109.1	125.3	172.3
DIBL (mV/V)	308	311	312	314	314

Figure 4 clarifies the characteristics of the electric field. The integration of HfO_2 SELBOX at a depth of 30 nm markedly diminishes fringing fields adjacent to the drain side, while the high-k shielding action of the oxide effectively obstructs field lines above the SELBOX. As the SELBOX approaches direct contact with the drain, the confinement of the electric field enhances, resulting in less vertical field penetration into the substrate. Nevertheless, robust localized electric fields develop within the SELBOX layer, aligning with the noted rise in I_{OFF}. This indicates that although HfO_2's elevated dielectric constant enhances isolation, its reduced bandgap renders it more vulnerable to field-assisted leakage mechanisms in comparison to SiO_2 or Al_2O_3 SELBOX.

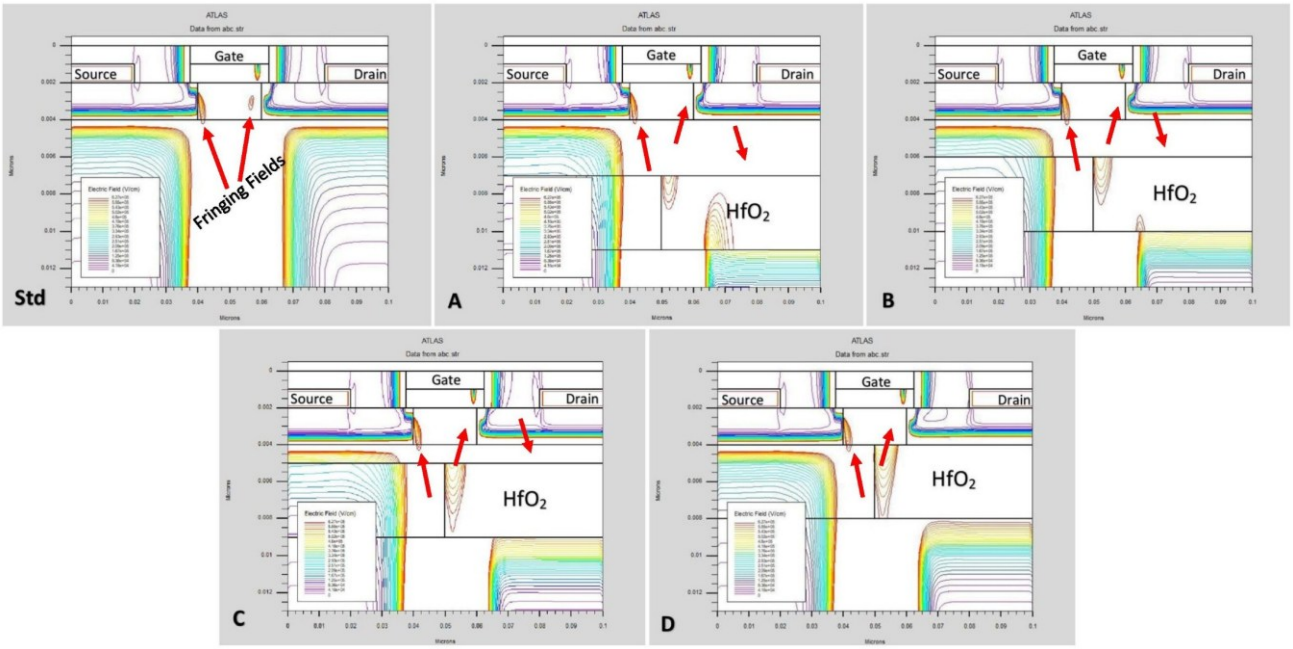

Fig. 4. Electric field distribution at (standard design of n-MOSFET) and HfO_2 selective buried oxide layer (SELBOX) at (30 nm depth, 20 nm depth, 10 nm depth and direct contact position).

4. Conclusion

Implanting a SELBOX beneath of drain region with three different materials, SiO_2, Al_2O_3, and HfO_2, with energy gaps of 9 eV, 8.8 eV, and 5.8 eV, respectively. The value of energy gap of materials and its closeness to drain region determines the average increasing and decreasing value of leakage current and breakdown voltage, as the SELBOX positioning from 30 nm depth to direct contact, it was noticed when the high value of band gap, such SiO_2 with 9 eV, and become more close to the drain-substrate contact, the leakage current is exponentially decreased by 17%, and the breakdown voltage is exponentially increased by 52%. When the band gap is slightly decreased, such as Al_2O_3 with 8.8 eV, the leakage current is slightly exponentially decreased by 10%, and the breakdown voltage is exponentially increased by 29%. Finally, the significant decrease in the value of band gap, such as HfO_2 with 5.8 eV, the leakage current is exponentially increased by 17%, and the breakdown voltage is exponentially increased by 16%. It was concluded that the material with a higher value of the band gap and closer to the drain region gives better results. Future research can extend this work in several directions, like exploring alternative high-k and ultra-wide band gap dielectrics such as ZrO_2, La_2O_3, or Ga_2O_3 as SELBOX layers could provide further insights into material-dependent performance. Another future approach, applying the concept of buried dielectric engineering to advanced device architectures, including FinFETs, Gate-All-Around (GAA) FETs, and nanosheet transistors, may reveal its scalability to beyond-20 nm nodes.

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