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Simulation Analysis of CMOS Device Fabrication Using Silvaco TCAD: Process Optimization for Biomedical Applications

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Abstract

This paper describes a detailed simulation of CMOS device manufacturing using Silvaco TCAD software. The simulated CMOS devices reached the final source/drain doping density of about $7x10^{19}$ cm^{-3} in both NMOS and PMOS devices, and the threshold voltage of about ±1 V, which can be used in many logic applications. N-well and P-well pre-annealing concentrations were $2x10^{17}$ cm^{-3} and $6x10^{17}$ cm^{-3} respectively with post drive-in diffusion depths of 2-3 μm. The LOCOS process was able to generate 0.5 μm field oxide to isolate devices. This paper offers specific information on process parameter selection and optimization and shows that process simulation is valuable in exhibiting fabrication-device characteristic relations. Moreover, the paper explains the CMOS fabrication infrastructure in biomedical sensor applications, in which CMOS technology has demonstrated notable potential biosensors, point-of-care diagnostics, and implantable medical devices.

Keywords: CMOS Fabrication, Silvaco TCAD, Biosensors.

1. Introduction

Complementary Metal-Oxide-Semiconductor (CMOS) technology has dominated the fabrication technology of integrated circuits through its low power consumption, high density of integration, and its high noise immunity over several decades [1, 2]. The history of constant scaling of CMOS devices has made more complex and powerful electronic

systems possible in a wide range of applications. Fabrication of the specific fabrication process is vital to ensure the optimal operation of the device and adjust the technology to meet the new applications. Technology Computer-Aided Design (TCAD) tools have been developed to become an inseparable part of the semiconductor device development process through process simulation [3, 4].

Simulation enables researchers and engineers to simulate complicated fabrication sequence, predict device behavior, and optimize design critical process parameters at much less cost and time than the physical runs of complex process fabrication. This ability has found specific application in educational environments to gain profound insight into understanding process-device interactions as well as understanding new device structures. In addition to conventional digital and analog integrated circuits, CMOS technology has had widespread use in biomedical devices and biosensors [5, 6].

The capability of combining the sensing components with the signal processing circuits on top of a single chip generates enormous benefits in three areas that include miniaturization, cost savings, and portability requirements mainly to point-of-care diagnostic devices and implantable medical devices [7,8]. CMOS based biosensors are highly sensitive for in vitro diagnostics, detecting concentrations as low as one attomolar DNA and femtomolar proteins [9].

The present paper provides a detailed simulation of the CMOS devices manufacturing with Silvaco Athena process simulator. All critical steps in fabrication including substrate preparation until the final step of forming sources/drains are covered with a detailed consideration of process parameter choices and optimization.

The simulated devices contain not only NFET transistors, which are also called NMOS, but also PMOS transistors within a twin-well CMOS architecture. It also provides guidance on how the processes of fabrication and device designs presented in this work are connected to biomedical biosensing applications based on recent work in CMOS biosensors and lab-on-chip systems.

2. Methodology

2.1 Simulation Platform and Approach

All simulations were carried out with Silvaco Athena, a full two-dimensional process simulation environment that simulates the major physical processes of semiconductor fabrication including ion implantation, diffusion, oxidation, etching, and deposition [10]. Doping profiles, junction depths, and geometries of devices can be predicted with great accuracy using this simulation environment.

Numerical methodology applied in a mesh format was used to generate suitable refinement in sensitive areas that guarantee accuracy at the cost of computation efficiency. The mesh was characterized by increased density around surfaces and junctions where sharp concentration gradients exist.

2.2 Substrate Formation

The CMOS manufacturing process started by utilizing substrate definition and initialization. A p-type doped silicon substrate with 100 crystal orientation was chosen with a concentration of boron doping of $1x10^{15}$ cm^{-3}. Such concentrations yield 25-50 Ω-cm resistivity that is suitable in CMOS applications and offers sufficient substrate conductivity with a high level of junction isolation [11].

The 100 orientations have been selected due to its superior electrical properties at the interface of Si/SiO_2. In fact, it has been demonstrated that such an orientation has a lower number of unsatisfied bonds than any other crystal orientations, which leads to a reduced interface state density and improved device performance [12]. In (figure 1) one can observe the original definition of the substrate and the mesh.

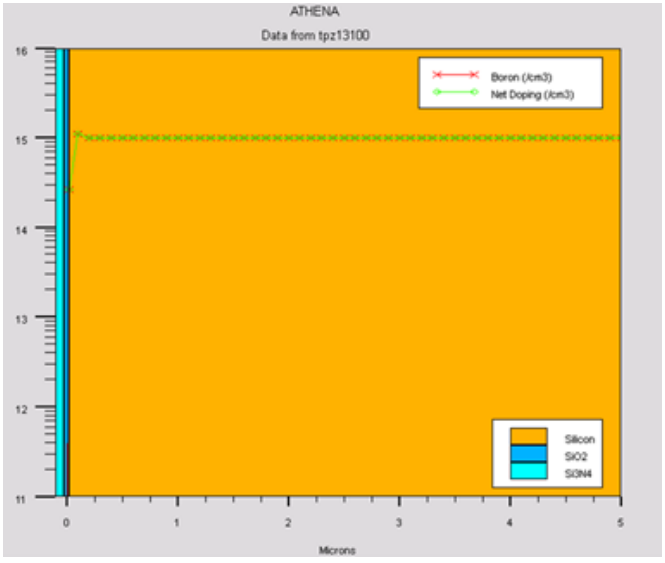

Figure 1: Formation of silicon 100 substrate with 1x1015 cm-3 boron doping (p-type).

2.3 Local Oxidation of Silicon (LOCOS)

The Local Oxidation of Silicon (LOCOS) process was used to obtain device isolation because it is a common method of producing field oxide areas between active devices [13]. The procedure started by depositing silicon nitride (Si_3N_4) that measured 0.08 µm in thickness. This oxidation mask is formed by a nitride layer which is fundamentally resistant to oxygen and water vapor at normal oxidation temperatures. Photolithography and dry etching were then used to pattern the nitride to create the active device features.

The Oxidation of LOCOS was conducted at 1100°C with wet O_2 ambiance, where it was allowed to grow about 0.5 µm field oxide within the 90-minute period. Wet oxidation was chosen due to the significantly high oxide growth rates in wet oxidation relative to dry oxidation [14]. The nitride layer was removed after the formation of LOCOS. The LOCOS sequence is represented in figures 2-4.

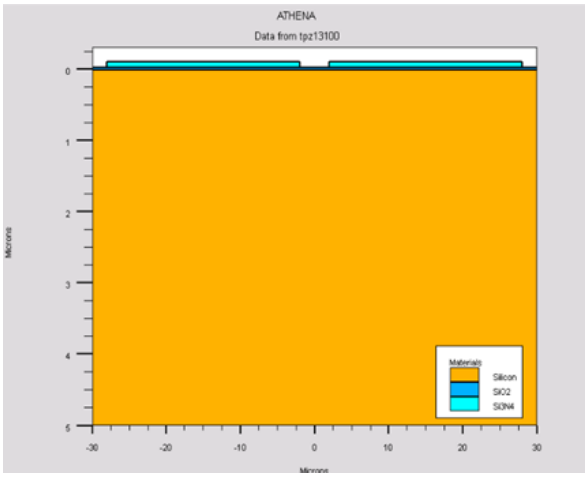

Figure 2: Nitride deposition (0.08 µm).

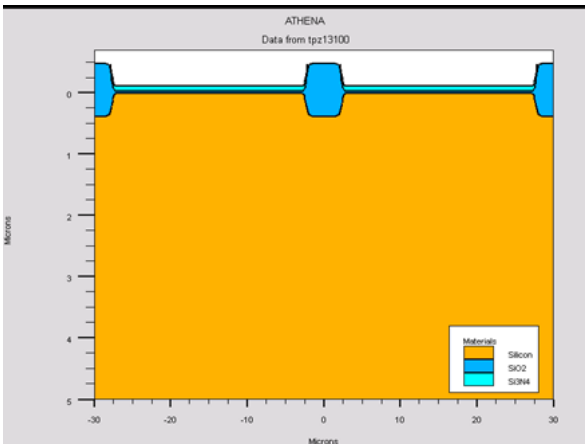

Figure 3: Nitride patterning and etching.

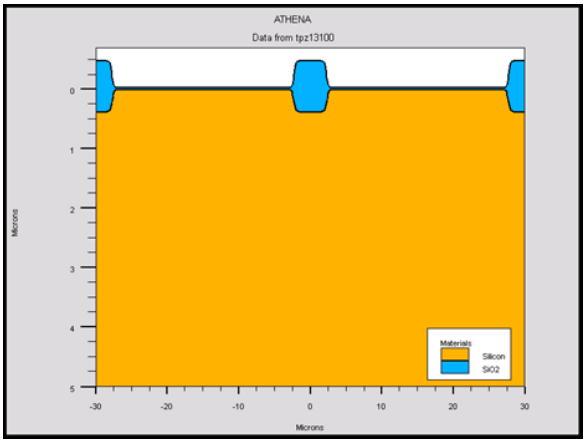

Figure 4: LOCOS formation with 0.5 µm field oxide.

2.4 Twin-Well Formation

The formation of twin-wells was achieved via sequential ion implantation and high-temperature diffusion. CMOS of twin-well involves the foundation of n-type and p-type wells. In case of the p-well, implantation was carried out using an energy of 150 keV at 2 x 10^{13} cm^{-2} of boron. In the case of the n-well, 350 keV phosphorus was implanted at a rate of 2x10^{13} cm^{-2}. Since the atomic mass of phosphorus is high compared to boron, it has varying implantation and diffusion properties compared with silicon [15].

After implantation, a drive-in diffusion was carried out at 1100°C using a diffusion time of 360 minutes to obtain well depths of 2-3 µm. Phosphorus was used to produce n-wells since it is an n-type dopant with appropriate diffusivity to create deep and uniforms wells. [17]. Figures 5-8 indicate the procedure of well implantation and annealing.

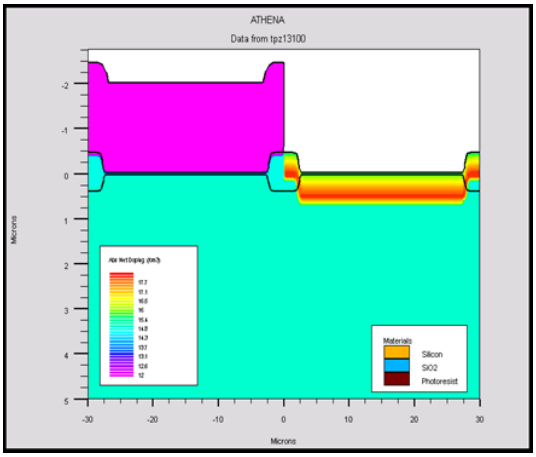

Figure 5: Boron insertion with 2x$10^{13}$$cm^{-2}$ at 150kev to form p-well.

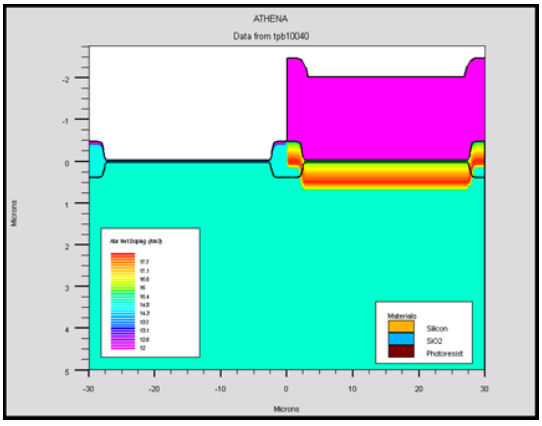

Figure 6: Phosphorus insertion with 2x10^{13} cm^{-2} at 150kev to form n-well.

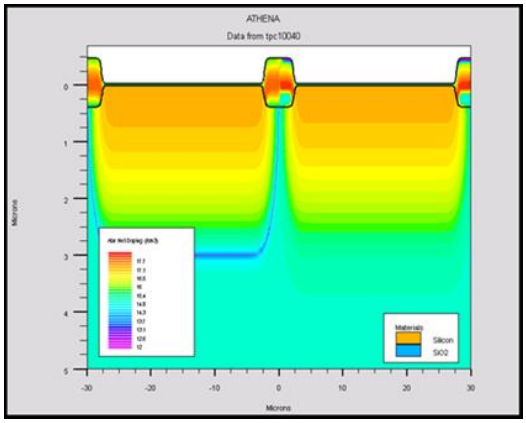

Figure 7: The profiles of wells after annealing.

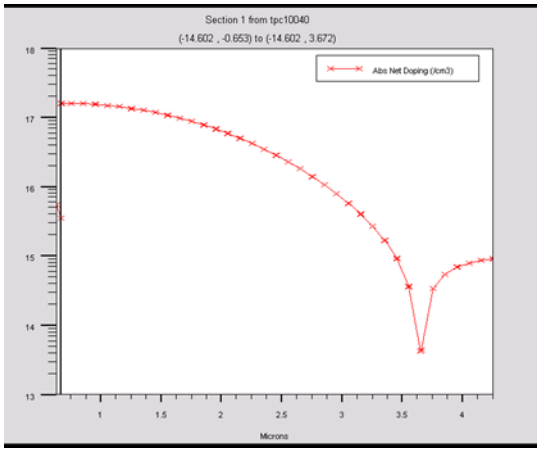

Figure 8: (a) Post drive-in profile of well (1100 °C, 360 min).

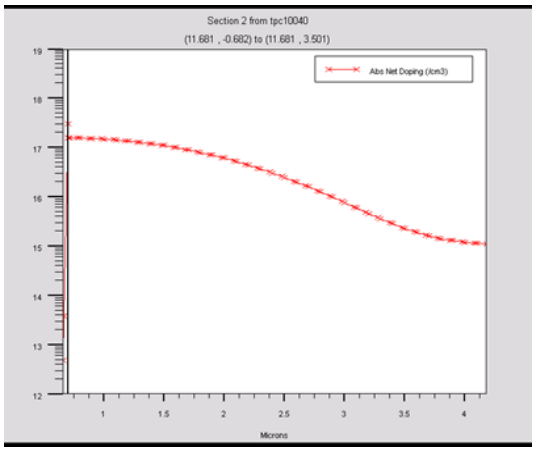

Figure 8: (b) N-well phosphorus profile.

2.5 Gate Oxide and Threshold Voltage Adjustment

Field oxide was removed from active regions after well formation. Approximately 10 nm oxide was produced by the growth of a thin gate oxide with dry O_2 at 800°C for 120 minutes [18]. Threshold voltage trimming was ensured with arsenic of $3.34x10^{11}$ cm^{-2} at 400 keV (NMOS) and boron of $1.496x10^{12}$ cm^{-2} at 40 keV (PMOS). The threshold voltages were set to ±1 V [19] that are standard values to CMOS logic applications. Figures 9-10 show this process.

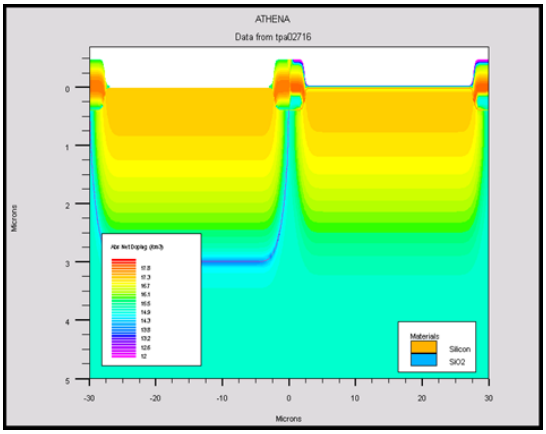

Figure 9: Gate oxide striping and regrowth (10 nm).

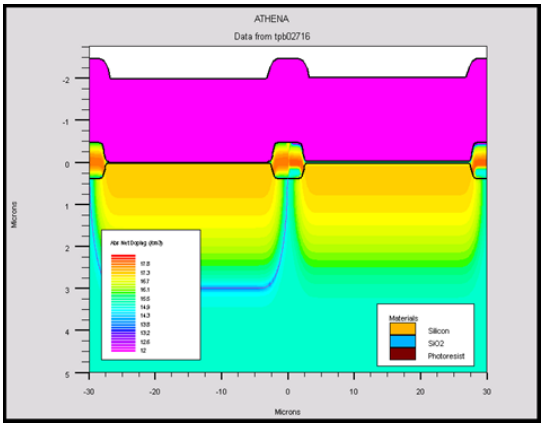

Figure 10: Implants of threshold voltage adjustment.

2.6 Polysilicon Gate Formation

The polysilicon gates (0.5 µm) were deposited and doped with phosphorus $1x10^{15}$ cm^{-3} and patterned by dry etching [20]. Figure 11 reveals the structure of poly gate.

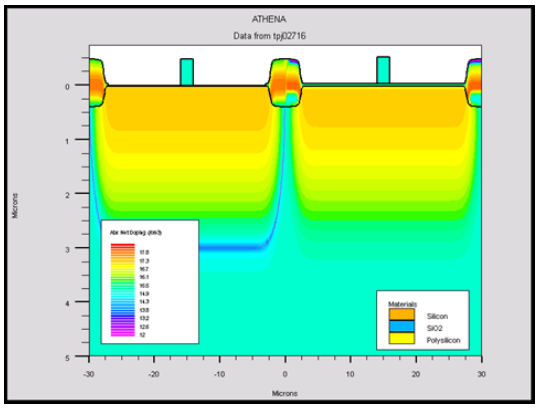

Figure 11: Poly silicon gate formation and patterning (0.5 µm).

2.7 Lightly Doped Drain (LDD) Formation

LDD designs reduce the effects of hot carriers [21]. In the case of NMOS LDD, phosphorus was implanted with $5x10^{13}$ cm^{-2} at 100 keV. In the case of PMOS LDD, Boron was implanted with $5x10^{13}$ cm^{-2} at 50 keV. Dopants were activated by a low temperature anneal at 1000°C for 60 minutes. Figure 12 presents the LDD implants.

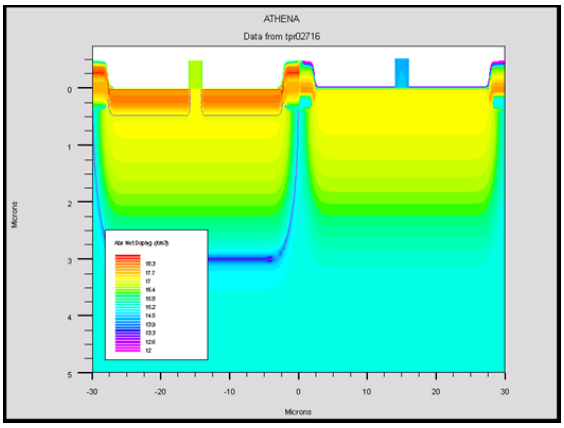

Figure 12: Photo of LDD (Lightly Doped Drain) implantation with lightly doped areas (orange/red) aligning to edges of the gate made of polysilicon.

2.8 Sidewall Spacer and Source/Drain Formation

Deposition and anisotropic etching were used to create oxide spacers (0.3 µm) [22]. The formation of the sources/drains involved the use of arsenic with $3x10^{15}$ cm^{-2} at 75 keV during the formation of NMOS and boron with $3x10^{15}$ cm^{-2} at 8 keV during the formation of PMOS [23]. The devices were finished with final activation anneal at 900°C in 30 minutes. Boron has lower energy which is due to its lower mass and a tendency to form shallow junction. The final structure is indicated in figures 13-14.

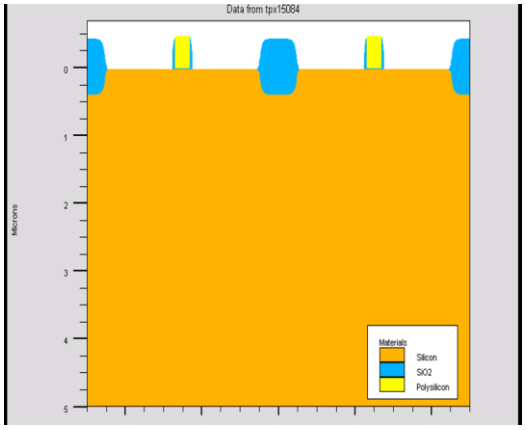

Figure 13: Final structure of CMOS device.

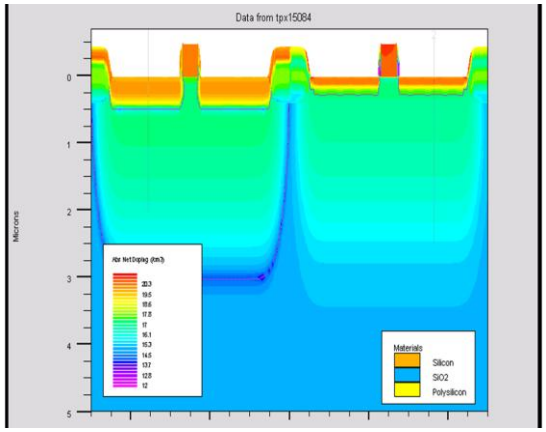

Figure 14: CMOS with junctions' boundaries

3. Results and Discussion

3.1 Device Structure and Doping Profile

The CMOS simulation has managed to yield both the NMOS and PMOS transistors with the correct doping profile. The ultimate source/drain doping levels were about $7x10^{19}$ cm^{-3} and were used to provide low series resistance. The final doping profiles of NMOS and PMOS devices are presented in the figures 15-16.

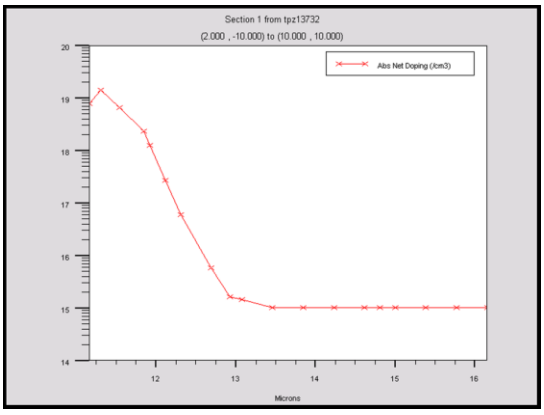

Figure 15: NMOS source/drain doping profile with final concentration estimated at $7x10^{19}$ cm^{-3} obtained by arsenic implantation ($3x10^{15}$ cm^{-2}, 75 keV) and activation anneal.

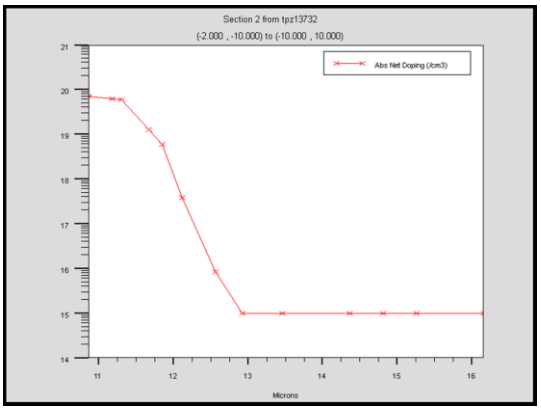

Figure 16: PMOS source/drain doping profile with final concentration of about $7x10^{19}$ cm^{-3} obtained after Boron implantation ($3x10^{15}$ cm^{-2}, 8 keV) and activation anneal.

3.2 Well Profiles

The concentration of the n-well was about $2x10^{17}$ cm^{-3} and the concentration of the p-well was $6x10^{17}$ cm^{-3} before annealing. The depths of both wells were 2-3 μm after drive-in diffusion at 1100°C for 360 minutes.

3.3 Isolation and Threshold Voltage

The LOCOS field oxide reached a thickness of about 0.5 μm which offered valuable isolation. The thickness of the gate oxide was about 10 nm. Threshold voltage adjustment implants are successful in adjusting the device threshold voltages to a range of ±1V in NMOS and PMOS devices.

4. Potential Biomedical Applications

Although the CMOS devices modelled in the study were developed as general-purpose transistors, the fabrication procedures and device design have important applications in biomedical fields. In fact, the development of biosensors using CMOS technology has been a challenging technology platform because of a few factors. These factors include low-cost mass production through existing semiconductor manufacturing, low power consumption allowing portable and implantable devices, and the possibility of integrating sensing components and signal processing circuits on a single chip [24, 25].

CMOS biosensors have already shown the capability of in vitro diagnostics with detection sensitivities of 10 attomolar in the case of DNA, 10 femtomolar in the case of proteins, and even single cell-detection sensitivity in bacteria detection [9].

These outstanding detection limits compete with or surpass standard laboratory methods with important miniaturization and time to result benefits. CMOS biosensors may utilize many different transduction principles such as potentiometric sensors that can be ion-sensitive field-effect transistors or ISFETs, amperometric sensors that sense changes in electrical current, impedimetric sensors which sense changes on electrical impedance, and optical sensors which use CMOS image sensors technology [26].

Fabrication processes presented in this work, in particular, the accuracy of doping profiles, the thickness of

oxides, and threshold voltages, are applied directly to the development of ISFET biosensors. ISFETs represent MOSFETs having the ion-sensitive membrane as their gate in direct contact with the analyte solution so the quality of the gate oxide and the ability to control threshold voltage experimentally as in conventional CMOS fabricated technologies have a direct application to sensor operation [27].

In addition to sensing in vitro, CMOS technologies can be adapted to implantable biomedical systems because of their very small size and very low power consumption required by new fabrication techniques [28]. Their applications include retinal prostheses to restore vision to individuals with degenerative retinal diseases, brain-implantable computers to record neural activity and complex neural interface circuits to use as close-loop neuromodulated systems.

Recent developments have shown CMOS based biosensors with thousands of microelectrodes to record neural activity in high spatiotemporal resolution allowing previously unachievable spatiotemporal resolution of brain activity and neural plasticity [29]. These advanced implantable systems are directly made possible by incorporating the vast quantities of transistors on a miniature chip shown by the CMOS fabrication processes in this research. Developing the standard CMOS fabrication for biosensor usage involves a series of post-processing changes.

First, CMOS electrode layouts require post-CMOS electrode depositions since common aluminum metallization cannot be used to contact cellular material, and instead the use of noble metals like platinum and gold or biocompatible materials like titanium nitride is required to be deposited on closed regions of the device [30]. Second, the sensor surfaces should be modified with suitable biorecognition factors such as antibodies, enzymes, or DNA probes by using the techniques of surface chemistry such as self-assembled monolayer, silanization, or polymer coverings [31].

Third, full lab-on-chip systems need microfluidic integration of sample manipulation, which may be achieved by bonding independently produced microfluidic layers, or by direct-write procedures on the CMOS chip [32].

Lastly, electronics must be encapsulated in proper packaging and be bio-compatible with encapsulation using material like medical-grade silicone or parylene to ensure the protection of electronics without inducing tissue reactions and corrosion in implantable applications [33]. Those modifications include the post-CMOS designs that are built using the accuracy of the device structures and the device fabrication procedures exhibited in this study and incorporating the dedicated functionalities needed in biomedical sensing.

5. Conclusion

This work has demonstrated a detailed process simulation of CMOS device manufacture based on Silvaco TCAD tools including the entire process cycle of substrate fabrication up to the development of finished devices. The simulations were able to showcase all the key process steps such as LOCOS isolation, twin-well formation, gate oxide development, threshold voltage optimization, polysilicon gate development, LDD development, and source/drain development. The resulting devices were of target specifications and had source/drain doping concentrations of around $7x10^{19}$ cm^{-3} in both NMOS and PMOS transistors, and threshold voltages in the order of ±1 V. During well formation, n-well and p-well areas were properly doped with $2x10^{17}$ cm^{-3} and $6x10^{17}$ cm^{-3}, respectively. Moreover, they had a depth of 2-3 μm following drive-in diffusion. The LOCOS was able to fabricate 0.5 μm field oxide to provide efficient isolation of devices.

The analysis of the process parameters indicates clearly that TCAD simulation is valuable in the research of relationships between fabrication-device characteristics and optimization of crucial parameters. This model of simulation allows effectively learning the process variability without costly fabrication. The application in biomedicine described herein indicates the wide potential of CMOS technology in non-IC applications. By implementing suitable post-processing changes such as biocompatible electrode formation, surface functionalization, and microfluidic integration, standard CMOS manufacturing processes can be modified to produce powerful biosensing platforms in medical diagnostics and implantable devices.

6. References

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