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COMPARISON OF TOTAL HARMONIC DISTORTION (THD) IN THREE-LEVEL, THREE-PHASE INVERTERS USING CASCADED H-BRIDGE (CHB) AND NEUTRAL-POINT-CLAMPED (NPC) TOPOLOGIES

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ABSTRACT

Utilizing the same parameters for operation, 50 Hz frequency, and 380 V line voltage, every single inverter is represented mathematically on the MATLAB/Simulink environment. The shape of the generated voltage's harmonics is examined using Fast Fourier Transform (FFT) approaches. The results demonstrate the benefits and drawbacks of each design by taking into account the THD values for each examined inverter with the exact same applied frequency and supply voltage. This paper uses modelling to analyse three-phase, three-level (CHB) and (NPC) inverters. Total harmonic distortion (THD), pattern efficacy, and structural complexity are all examined. Simulation findings show that the NPC architecture needs fewer DC sources and is simpler to control, whereas the CHB inverter generates less THD (~4.7%) compared with the NPC architecture (~9.2%). Because they provide better waveforms, less acoustic noise, and less switching strain, inverters that have less harmonic distortion are favoured in medium- and high-power applications.

KEYWORDS

CHB, NPC inverters, THD, and MATLAB/Simulink modelling.

1. INTRODUCTION

In order to enhance the solar photovoltaic (PV) connected to the grid procedure, a novel 15-stage inverter is introduced in the article. Having a voltage THD of 15.77% and a current THD of 3.91%, the waveform patterns' accuracy greatly improved. The design's performance allows it to reach a 96.75% power conversion effectiveness level. (E. Parimalasundar, R. Senthilkumar, R. Jayanthi. (2025). In renewable energy systems where multilayer inverters (such as NPC and CHB) are crucial for network integration, the present research investigates control techniques. It examines the effects of various algorithms for control on the conversion system's loss of operation and quality of power (THD) under various workload scenarios. Al-Jabari, A., et al. (2022). Due to their suitability for moderately and high-voltage usage, inverters with multiple levels have grown in demand over time. The reason for this research is that, in comparison to traditional two-level inverters, they can produce massive AC (alternating current) results with lower Total Harmonic Distortion (THD), less switching tension on equipment, and higher efficiency (Al-Khayyat, H., Rahman, S., & Uddin, M.N., 2024). However, it has some positive drawbacks, such as a greater variety of components and voltage unevenness at the neutral aspect (Sahoo, S. and Kar, A. 2023; Nguyen, H.T. and Lee, D.C. 2022).

However, the CHB inverter is a beautiful concept for grid interface and green electric systems since it utilises several H-bridge components connected to one of the type DC supplies. This enables advantages including increased adaptability, dependability, and simplicity of expansion (Prabaharan, N. and Palanisamy, K. 2021; Mondal, S. and Banerjee, S. 2021). Every NPC and CHB inverter must strive for THD minimisation. The basic compromise in NPC (diode-clamped) topologies is investigated in this work. The increasing number of semiconductors usually results in higher prices and losses in switching as voltage levels rise. In contrast to conventional NPC topologies, it suggests an altered five-level architecture intended to boost performance by lowering the switch count, which immediately reduces the overall switching losses and improves the THD. Anssari (2021). The study compares Level-Shifted PWM (LS-PWM) and Level-Phase-Shifted PWM (LPS-PWM), both of which are essential to both NPC and CHB inverters, while concentrating on switching-capacitor architectures. The results show that LPS-PWM outperforms LS-PWM, particularly when it comes to lowering the output voltage's THD. Abdul-Abbas, A., and Salih, S. (2021). Prediction management and other high-order control methods have been proposed to lower THD and improve the dynamic responsiveness of these kinds of inverters (Khan, M.A. and Zafar, F. 2020; Mondal et al. 2021). THD is an important indicator of the output pattern accuracy of these inverters (Al-Hussain and Hamad, 2023). Based on the findings, when paired with the most effective available modulation

techniques like SPWM, SVM, or SHE, both the CHB and NPC architectures can provide remarkably lower THD values than two-level inverters (Kouro et al. 2010; Franqueloet al. 2008). Using the framework's prediction control utility, three-level structures have been further enhanced seamlessly (Patel, H. and Agarwal, V. 2006). Two of the most researched inverter architectures for three-level systems are NPC and CHB. By using clamping diodes to divide the DC bus into multiple stages, the NPC inverter, which first appeared in the 1980s, enhances waveform stability and lessens changing stress caused by voltage (Dekka et al. 2017). Two challenges with the design are the impartial element voltage equilibrium and the inclusion of additional elements as the voltage levels increase, resulting in jostling (Babaei et al. 2014). On the other hand, the CHB inverter supplies a range of voltage levels by connecting H-bridge cells in sequence, each of which has a distinct DC electricity source. The increased versatility, adaptability, and reliability of this modular structure can be advantageous for equipment that employs readily available energy sources, such as daylight and a battery-based platform (Malinowski et al. 2010).

1.1. Novelty and Contributions

However, the need for multiple distinct DC sources may make the sketch more difficult in practical applications. The novelty of this work is thoroughly explained in the preface and Conclusions. The distinctive advantage of this research resides in; a tracked, continuous THD evaluation utilizing equal operational variables (380 V line-to-line, 50 Hz, similar modulation method, and switching frequency) in spite of the well-known CHB and NPC inverter topologies. A uniform MATLAB/Simulink simulation framework is able to separate topology-dependent harmonic activity. The original information presently in print sometimes lacks a relevant focus on results evaluation aimed at medium-voltage three-phase uses, emphasising control techniques over topology-level evaluation.

2. RESULTS AND DISCUSSION

Fig. 1 shows the single-phase A connection for a three-level NPC inverter. It displays a three-level, single-phase NPC leg with switches S1 through S4, a split DC link (C1, C2), and clamping diodes D1 and D2 connected to the neutral point. We require the line-to-line 380 V at 50 Hz, the 380 V L voltage, and the relationship between the DC bus and AC RMS output to compute the DC voltage. Therefore, 220 V rms per phase is equal to the single-phase. Each NPC leg in a sinusoidal half-bridge architecture has a basic peak voltage of V phase, peak (Vdc/2). Consequently. As may be seen below, the total Vdc for 220 V is approximately 622 V. The split capacitors would then each reach Vdc = ±311 V, which would allow them some margin for ripple and component tolerances. The output levels for each leg are Vdc/2, 0, and -

Vdc/2. The modulation technique (e.g., SPWM vs. SVPWM) and switching frequency determine the switching losses and THD.

$$\text{V dc} = \frac{2\sqrt{2}*\text{Vph,rms}}{\text{M}} = \frac{2\sqrt{2}*220}{1} = 622 \text{ V, M} = 1$$

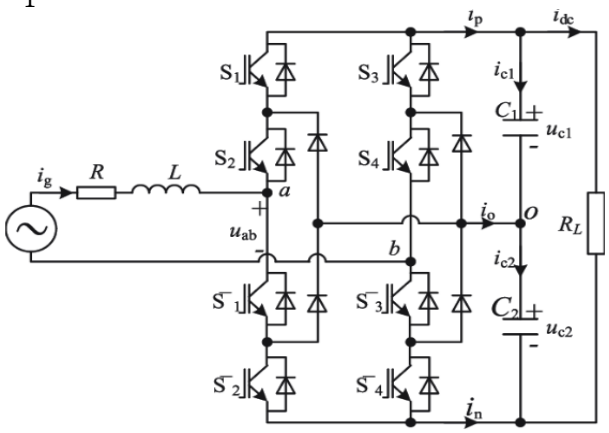

Fig. 1. Single-Phase Leg (3-Level NPC)

The various switch positions and the corresponding voltages (for each leg) at the load terminals for the voltage VAN are displayed in Table 1. When switches S1 and S2 are both on and switches S3 and S4 are both off, the voltage VAN at the load is + Vdc/2. If S1 is off, S2 is on, S3 is on, and S4 is off, the voltage VAN at the load is zero. When S1 and S2 are both off and S3 and S4 are both on, the voltage VAN at the load is negative, or Vdc/2. When there is no voltage, the diodes help keep the pole connected to the neutral point.

Table 1 Switching / Output States (per leg)

State	S1	S2	S3	S4	Pole voltage VAN
+Vdc/2	ON	ON	OFF	OFF	+Vdc/2
0 (via upper clamp)	OFF	ON	ON	OFF	0
−Vdc/2	OFF	OFF	ON	ON	−Vdc/2

2.1. Three-level three-phase Clamped Neutral Point (NPC) Inverter.

A three-level, three-phase Clamped Neutral Point inverter is depicted in Fig. 2. The DC bus rails are displayed as follows: +Vdc/2, Z Neutral (0), and −Vdc/2. A, B, and C are three legs. with four switches each (SA1–SA4 for A, SB1–SB4 for B, and SC1–SC4 for C). Clamping diodes that join the neutral line and the midpoint. Phase outputs (A, B, C) are connected to the motor

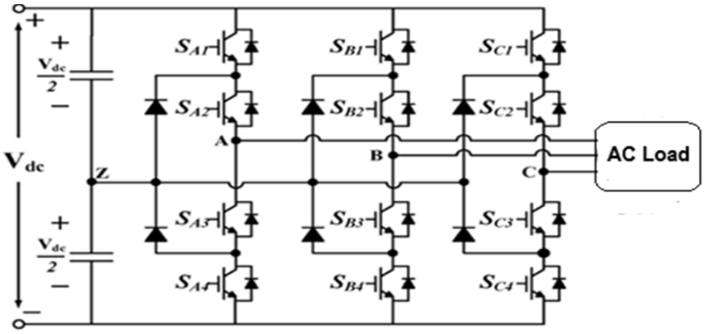

Fig. 2 displays a Neutral Point Clamped (NPC) inverter with three levels and three phases.

The NPC Switching time table per-leg switching patterns for Phases A, B, and C are displayed in Table 2 (columns A_S1 to A_S4, B_S to B_S4, and C_S1 to C_S4). The clamping diode conducts in each of the four basic leg states: +Vdc/2, 0 (upper clamp), 0 (lower clamp), and −Vdc/2. An annotated diagram displaying current/clamp-diode conduction paths for each leg state, a full 3-phase combined table listing line-to-line voltages (V_{AB}, V_{BC}, and V_{CA}) for every possible combination of per-phase states (i.e., $4^3 = 64$ rows), or an example PWM strategy (SVPWM or carrier-based) mapped onto these states with timing pulses.

Table 2 showing the three-level three-phase NPC Switching time table

hase	State	A_S1	A_S2	A_S3	A_S4	e_volta	amping/Diod	B_S1	B_S2	B_S3	B_S4	C_S1	C_S2	C_S3	C_S4
A	+Vdc/2	ON	ON	OFF	OFF	+Vdc/2	No diode (pole at +rail)								
A	0 (uppe	OFF	ON	ON	OFF	0	Upper clamping diode conducts (connects pole to neutral)								
A	0 (lowe	ON	OFF	OFF	ON	0	Lower clamping diode conducts (connects pole to neutral)								
A	-Vdc/2	OFF	OFF	ON	ON	-Vdc/2	No diode (pole at -rail)								
B	+Vdc/2					+Vdc/2	No diode (pc	ON	ON	OFF	OFF				
B	0 (upper clamp)					0	Upper clamp	OFF	ON	ON	OFF				
B	0 (lower clamp)					0	Lower clamp	ON	OFF	OFF	ON				
B	-Vdc/2					-Vdc/2	No diode (pc	OFF	OFF	ON	ON				
C	+Vdc/2					+Vdc/2	No diode (pole at +rail)					ON	ON	OFF	OFF
C	0 (upper clamp)					0	Upper clamping diode conducts (connect					OFF	ON	ON	OFF
C	0 (lower clamp)					0	Lower clamping diode conducts (connect					ON	OFF	OFF	ON
C	-Vdc/2					-Vdc/2	No diode (pole at -rail)					OFF	OFF	ON	ON

2.2. Single-Phase Cascaded H-Bridge (CHB) Inverter

A single-phase cascaded H-bridge (CHB) inverter is seen in Fig. 3, and its output levels will be as follows: 3-level waveform: -2Vdc, -Vdc, 0, +Vdc, +2Vdc. The output voltage levels are +Vdc, 0Vdc, and -Vdc (per H-Bridge) and are obtained by cascading two H-Bridge cells (each 3-level → combined 5 levels). Multiple H-Bridges can be cascaded to enable 5-level, 7-level, and 9-level.

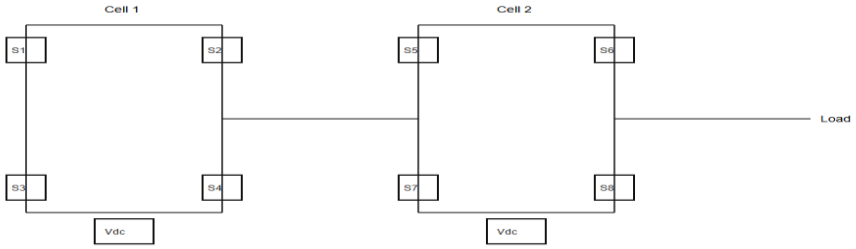

Fig. 3. displays an H-Bridge (CHB) inverter that is single-phase cascaded.

The operation (switching) table for a single-phase H-Bridge CHB cell is displayed in Table 3. There are four switches on each H-bridge: S1, S2, S3, and S4. The output voltage (Vo) across the load is determined by switching. The output from modes 1 and 2 is entirely positive or negative. When the load is shorted across the higher or lower path, modes 3 and 4 provide zero output. Multilevel voltages are produced when several series cascades of H-bridges, with the total output equivalent to the total of the Vo of each H-bridge:

Multilevel voltages are produced when several series cascades of H-bridges, with the overall

output equivalent to the total of the Vo of each H-bridge; for two cells, there are five levels (-2Vdc, -2Vdc, 0, +Vdc, +2Vdc, etc.); for three cells, there are seven levels, etc.

Table 3 Operation (switching) chart for an H-Bridge CHB cell in single phase

Mode	S1	S2	S3	S4	Output Voltage (Vo)
1	ON	ON	OFF	OFF	+Vdc
2	OFF	OFF	ON	ON	−Vdc
3	ON	OFF	OFF	ON	0 (short-circuit path)
4	OFF	ON	ON	OFF	0 (short-circuit path)

2.3. An H-Bridge (CHB) inverter with three levels and three phases of cascade.

Fig. 4 displays the following: There are three phases (A, B, and C) with two H-Bridge cells in cascade, each driven by a separate Vdc. S1–S24 switches are present in all three phases.

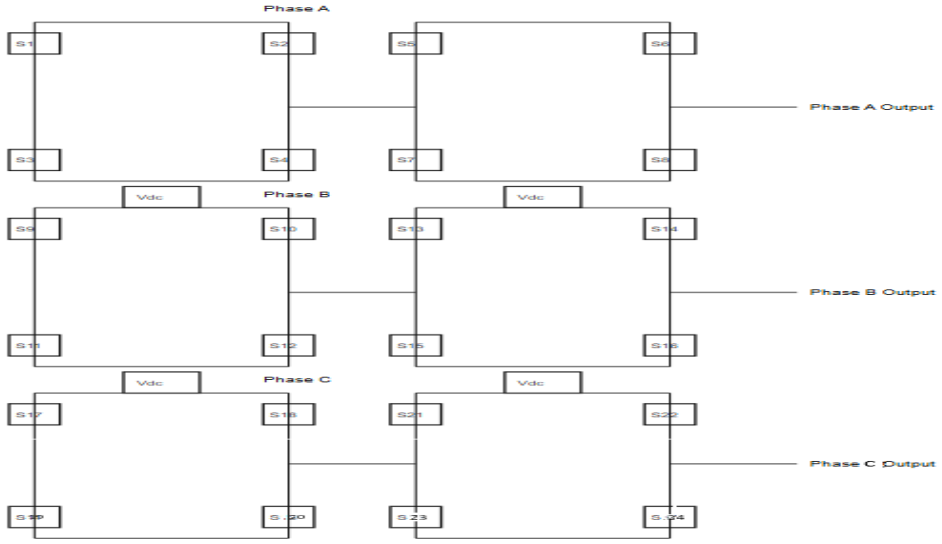

Fig. 4. displays a 380 V, 50 Hz, three-level, three-phase cascaded H-Bridge (CHB) inverter.

The whole switching/operation table for the CHB inverter with three levels and three phases, which includes two H-bridge cells cascading in each phase, is shown as below, the four switches used by each H-bridge cell (per phase) are left/top, right/top, left/bottom, and right/bottom. S1–S8 switches were utilized for Phase A: Top-left, top-right, bottom-left, and bottom-right cells in cell A1 are S1, S2, S3, and S4. Cell A2 cells are S5, S6, S7, and S8. Cell B1 S9–S12 and Cell B2 S13–S16 are the switches for Phase B. Cells C1 S17–S20 and Cell C2 S21–S24 are the switches for Phase C. The DC voltage of a single cell is denoted by Vcell; each cell has its own separate Vdc. The total of the cell outputs is the phase output (VAN, etc.). The output state of a single H-bridge cell (typical switching patterns), +Vcell: top switches (left and right top) are turned on. (ON, ON, OFF, OFF). 0 (upper clamp): OFF, ON, ON, OFF → right-top + left-bottom ON, 0 (lower clamp): ON, OFF, OFF, ON → left-top + right-bottom ON The bottom switches on (OFF, OFF, ON, ON) are the −Vcell. To balance neutral currents in your PWM scheme, dependably select one of the two acceptable zero states. Refrain from simultaneously activating both switches, leg (S1 & S3, for example).

Table 4 Reference for a single H-bridge (cell) switching (per cell)

Cell state	Switch pattern (top-left, top-right, bottom-left, bottom-right)	Resulting V_cell
+Vcell	ON, ON, OFF, OFF	+Vcell
0 (upper clamp)	OFF, ON, ON, OFF	0
0 (lower clamp)	ON, OFF, OFF, ON	0
−Vcell	OFF, OFF, ON, ON	−Vcell

The combined two-cell (per phase) switching table is displayed in Table 5. The per-phase voltage (Vphase = Vcell1 + Vcell2) and all possible combinations of the representative states of the two cells are listed in this table. Depending on which cell is +/0/−, you can collapse rows 2 and 4 to make + Vcell and rows 6 and 8 to produce − Vcell. Thus, +2·Vcell, +Vcell, 0, −Vcell, and −2·Vcell are the conceivable phase voltage levels. +2·Vcell, +Vcell, 0, −Vcell, and −2·Vcell are the possible phase voltage values.

Table 5 displays the combined two-cell switching table for each phase.

Row	Cell1 state	Cell1 pattern (Sx)	Cell2 state	Cell2 pattern (Sx)	Phase Vo
1	+Vcell	S_top pair ON (Cell1)	+Vcell	S_top pair ON (Cell2)	+2·Vcell
2	+Vcell	(Cell1)	0	(upper or lower) (Cell2)	+Vcell
3	+Vcell	(Cell1)	−Vcell	(Cell2)	0
4	0	(Cell1)	+Vcell	(Cell2)	+Vcell
5	0	(Cell1)	0	(Cell2)	0
6	0	(Cell1)	−Vcell	(Cell2)	−Vcell
7	−Vcell	(Cell1)	+Vcell	(Cell2)	0
8	−Vcell	(Cell1)	0	(Cell2)	−Vcell
9	−Vcell	(Cell1)	−Vcell	(Cell2)	−2·Vcell

Phase A is shown in Table 6. This useful table maps the ON/OFF switches for Cell A1 (S1–S4) and Cell A2 (S5–S8) to the Phase A pole voltage using the switch names as shown below. I only display one representative zero state in each cell for the sake of conciseness. Row 8 would have both cells −Vcell → −2·Vcell (both cells would have the pattern OFF OFF ON ON).

Table 6 The combined two-cell switching table is displayed in Phase A.

Phase-A index	S1	S2	S3	S4	S5	S6	S7	S8	v_AN
1 (+2Vcell)	ON	ON	OFF	OFF	ON	ON	OFF	OFF	+2·Vcell
2 (+Vcell)	ON	ON	OFF	OFF	OFF	ON	ON	OFF	+Vcell
3 (0)	ON	ON	OFF	OFF	OFF	OFF	ON	ON	0
4 (+Vcell)	OFF	ON	ON	OFF	ON	ON	OFF	OFF	+Vcell
5 (0)	OFF	ON	ON	OFF	OFF	ON	ON	OFF	0
6 (−Vcell)	OFF	OFF	ON	ON	OFF	ON	ON	OFF	−Vcell
7 (0)	OFF	OFF	ON	ON	OFF	OFF	ON	ON	0
8 (−Vcell)	OFF	OFF	ON	ON	OFF	OFF	ON	ON	−Vcell

Phases C and B replication, similar to Phase A. Phases C and B are covered by the same tables. Simply change their switch names: Cells B1 (S9–S12) and B2 (S13–S16) comprise Phase B. Cell C1 (S17–S20) and Cell C2 (S21–S24) comprise Phase C.

2.5: Total Harmonics produced by the two topologies CHB and NPC inverters.

The spectrum for a Neutral Point Clamped (NPC) inverter with three levels running at an RMS

voltage of 380 V is shown in detail in Figs.5 and 6. This figure compares and analyses Neutral Point Clamped (NPC) and Cascaded H-Bridge (CHB) distortion with total harmonics (THD) inverter setups. A thorough assessment of each inverter topology's harmonic performance is made possible by this simultaneous display, which also highlights each one's advantages and disadvantages with regard to THD levels. The capability to obtain particular information into the spectrum elements allows for a greater awareness of the impact that each inverter design has on overall power reliability.

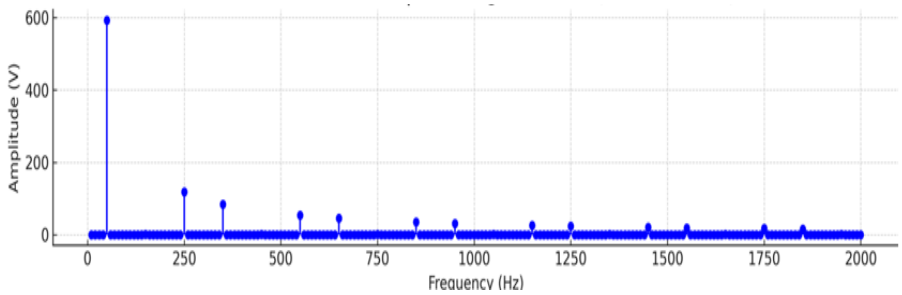

Fig. 5. 3-level NPC inverter spectrum at 380 V RMS

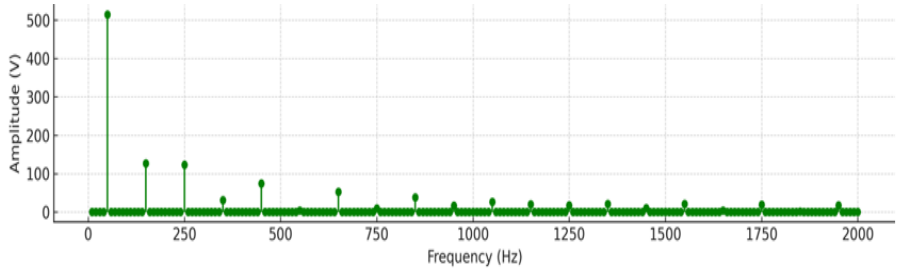

Fig. 6. shows the 3-level CHB inverter spectrum at 380 V RMS

2.4. Evaluation of CHB and NPC Topographies for Three-Level, Three-Phase:

Table 7 shows how CHB and NPC should be used based on their features and applications.

Table 7 The overall evaluation of CHB and NPC topographies for three-level, three-phase

Feature	CHB (Cascaded H-Bridge)	NPC (Neutral Point Clamped)
Output Waveform Quality (THD)	Lower THD (~4–8%) (Better)	Higher THD (~8–12%)
Flexibility & Modularity characteristics	(Better) Extremely configurable	Less modular
Changing the Number of Devices: Additional switching and separate supply	Changing the Number of Devices: Additional switching and separate supply	(Better) Fewer devices (centralised DC bus)
DC Supply Requirement	Several separate voltages are required	(Better) Single DC link
Control Complexity	More complex	(Better) Simpler
Fault Tolerance	(Better) Good (modular redundancy possible)	Less tolerant
Efficiency	(Better) High (due to lower switching losses)	(Better) High (but varies with load)
Cost	Higher (due to isolated DC and more parts)	(Better) Lower for small systems
Best for	Large/modular systems (e.g., renewables, drives)	Compact medium-power systems

3. CONCLUSION

- For a 50 Hz, 380 V (line-line) application; because of finer waveform structure using numerous H-bridges, and if you can manage isolated supply and your goal is reduced THD. CHB is superior. Also can work at decreased capacity while avoiding a malfunctioning H-bridge to meet the modularity & fault tolerance requirements, CHB is superior
- NPC is superior if you prefer a more straightforward design, a centralized DC supply, and a little greater THD. Also, if the objective of control & cost advantage, simpler creation of SPWM (Sinusoidal pulse width modulation) with fewer components. NPC is superior .
- Lastly, the comparison metrics based on the results of simulations on the NPC 3-level, three-phase inverters and the CHB topologies are as follows in Table 8:

Table 8 The comparison metrics according to the simulations on the NPC Versus CHB topologies

Metric	3-Level CHB	3-Level NPC
THD (%)	Around 4.7% (the lower the better).	~9.2% (greater)
Switching Frequency	2 kHz (that can be raised)	2 kHz
Voltage Steps	Three phases or steps	Three phases or steps
Total Losses	Because of modularity, it is lower	Overall, a little higher
Control Complexity	Greater (per H-bridge multi-carrier SPWM)	Lower (one carrier per leg of the phase)
DC_Bus Configuration	Six separate DC supplies are needed.	One DC link that is split

In this work, three-phase, three-level Cascaded H-Bridge (CHB) and Neutral Point Clamped (NPC) inverters operating at 380 V and 50 Hz are compared using modelling. The modulation and loading conditions for MATLAB/Simulink systems are the same. The investigation addresses the complexity of structure, pattern effectiveness, and total harmonic distortion (THD). According to simulation data, the CHB inverter produces lower THD (~4.7%) than the NPC architecture (~9.2%), and the NPC inverter requires less DC-source and has easier management.

4. RECOMMENDATIONS:

The following suggestions are put forth according to a comparison of the three-level Neutral Point Clamped (NPC) and Cascaded H-Bridge (CHB) inverters running at 380 V and 50 Hz. Either CHB or NPC to choose should depend on the specific requirements of the application; use the Cascaded H-Bridge (CHB) for situations where power quality is crucial. Because of its unusually low Total Harmonic Distortion (THD) of about 4.7%, high efficiency, and improved fault tolerance, the CHB architecture is recommended for grid-interfacing systems, high-power motor drives, and integration of renewable power, where distortion from harmonics must be eliminated. For applications where cost, space limits, and control simplicity are more important than harmonic performance, use Neutral Point Clamped (NPC). For compact medium-power

drives and industrial systems where a THD of around 9.2% is permissible within standard limits, the NPC inverter continues to be a reliable option due to its single DC-link requirement and easier maintenance.

Although this study offers a comprehensive modelling based on MATLAB/Simulink, it is highly advised that subsequent studies confirm these results by experimental implementation on hardware. To examine everyday events that models could miss, like the semiconductors' actual switching losses and thermal behaviour. element tolerances' effects on voltage balance, particularly with regard to the NPC neutral point. The high-frequency switching produces electromagnetic interference (EMI).

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